

MODEL NAME :ZAW12

PCB NO : LA-A691P

BOM P/N : DA60012B000 LA-A691P M/B

DA40001G410 LS-9105P POWER BUTTON/B

DA40001FP10 LS-9102P USB/B

DA40001FQ10 LS-9103P TP BUTTON/B

DA40001FR10 LS-9104P ODD/B

Dell / Compal Confidential

Schematic Document

AMD FP2 Richland Processor with DDRIII + Bolton M3 FCH

AMD VGA Sun XT

2013-05-23

Rev: 1.0

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

UMA@ : Only for UMA

DIS@ : Only for Discrete

GCLK@ : Green CLK implemented

NGCLK@ : Non Green CLK implemented

@3221: ALC 3221

@3223 : ALC 3223

EMC@ : EMC Parts

NEMC@ : EMC不上件

R1@ : R1 P/N for PCB

R3@ : R3 P/N for PCB

THR1@ : Thames-XT R1 P/N

THR3@ : Thames-XT R3 P/N

CHR1@ : Chelsea-Pro R1 P/N

CHR3@ : Chelsea-Pro R3 P/N

R@ : RTD2132-R

S@ : RTD2132-S

KBBL@ : KeyBoard Backlight

X76@ : VRAM Group

CH@ : Chelsea M2

SE@ : Seymour M2

TH@ : Thames-XT

Mars@ : Mars Pro M2

A4R1@ : A4 APU-R1

A6R1@ : A6 APU-R1

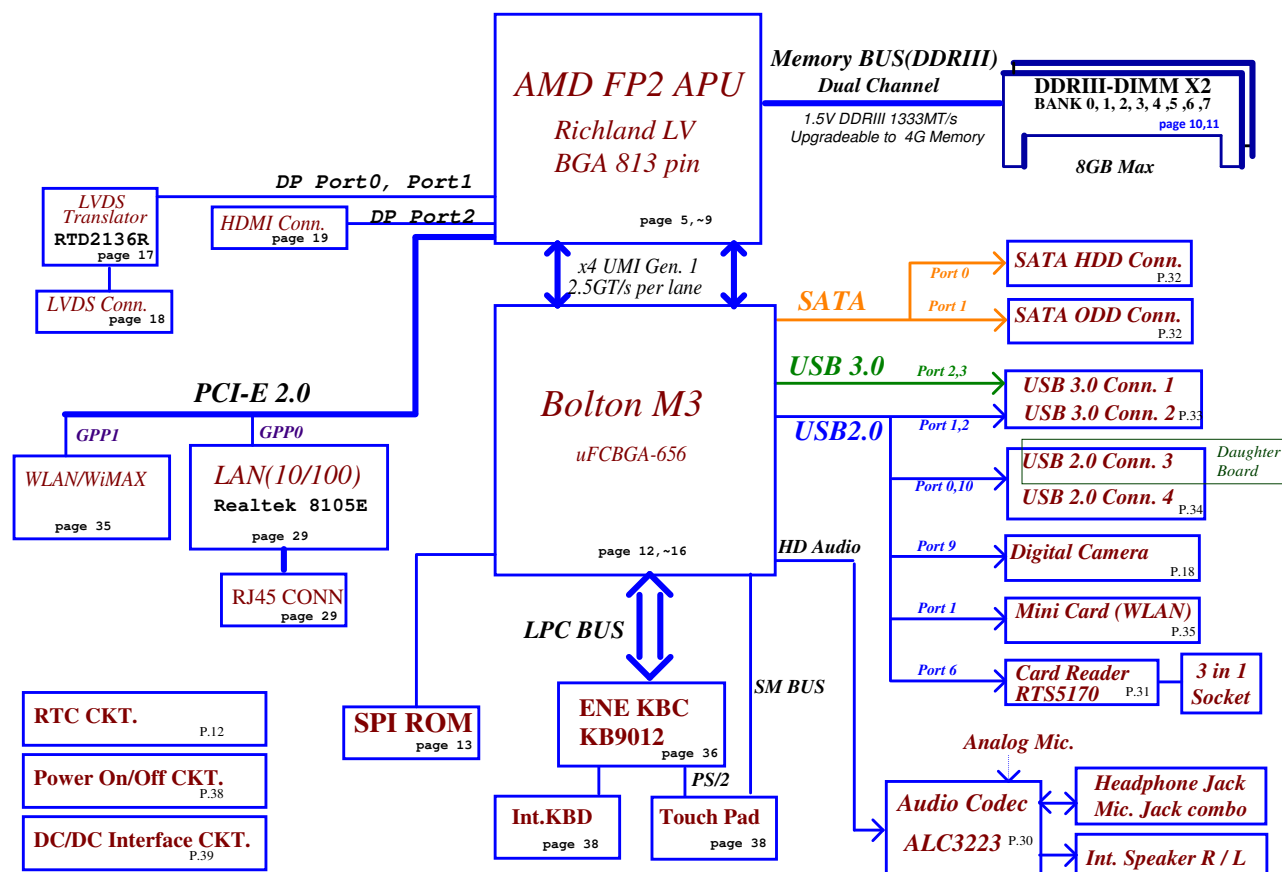
A8R1@ : A8 APU-R1

A8@ : A8 APU Symbol

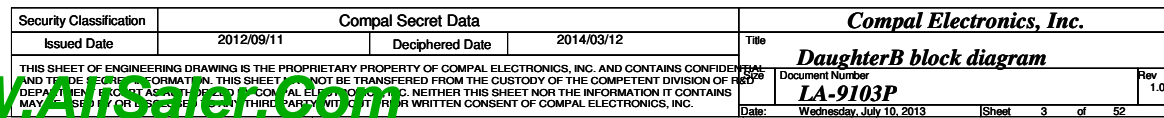
Hud@ : HUDSON-M3

Bol@ : BOLTON-M3

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Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0 SD028330280
4	
5	
6	
7	

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	000 1011	11h 0x16	ADM1032ARMZ	100 1101	4Dh 0x9A
Charger IC	000 1001	09h 0x12	SB-TSI	100 1100	4Ch 0x98
			RTD2132	100 1010	4Ah 0x94
			GPU	100 0001	41h 0x82

SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

Symbol Note :

 : means Digital Ground

 : means Analog Ground

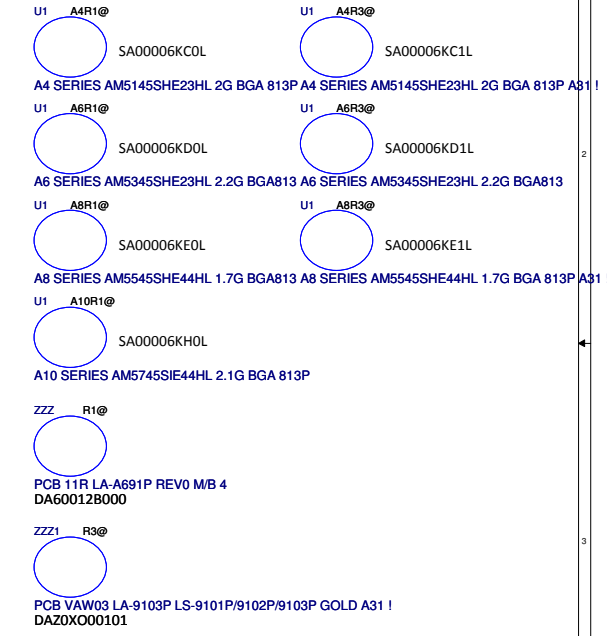
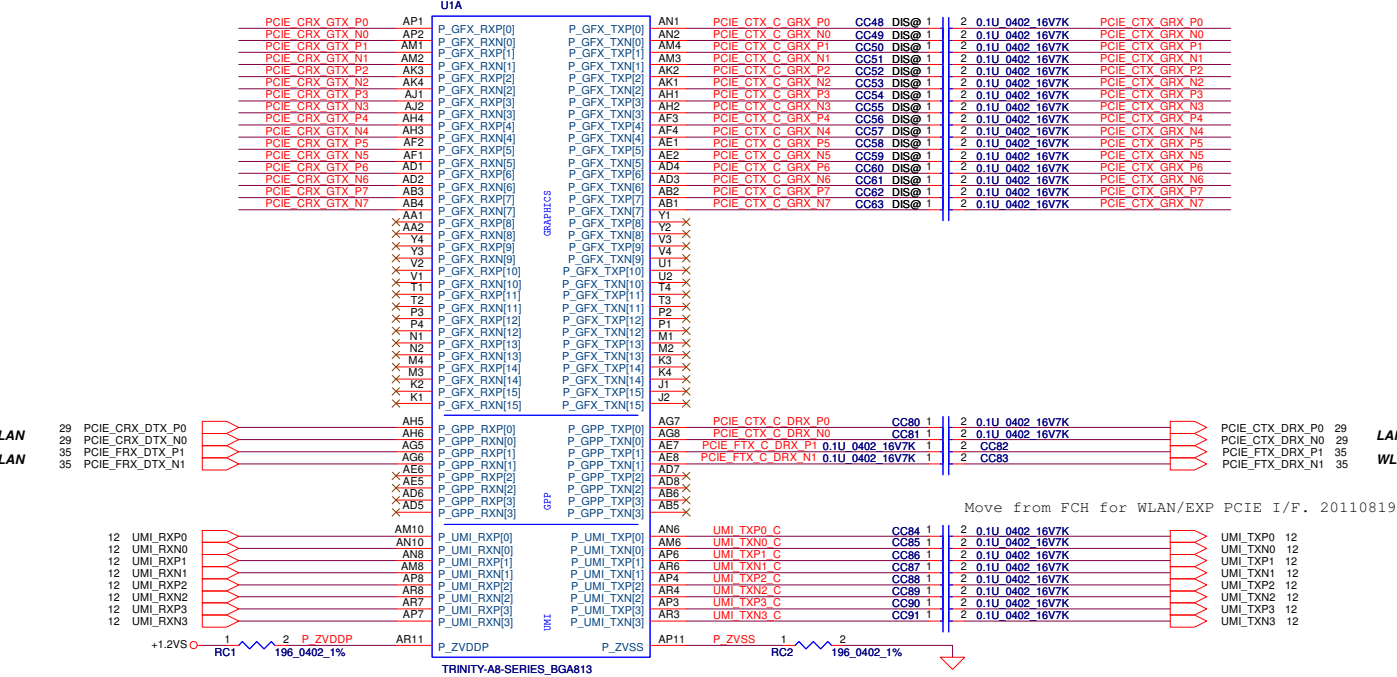
FCH

USB PORT#	DESTINATION
0	USB conn.3 DEBUG PORT
1	MINI CARD (WLAN)
2	USB conn.4
3	NC
4	NC
5	NC
6	Card Reader
7	NC
8	NC
9	Camera
10	USB conn.2
11	NC
12	NC
13	USB conn.1

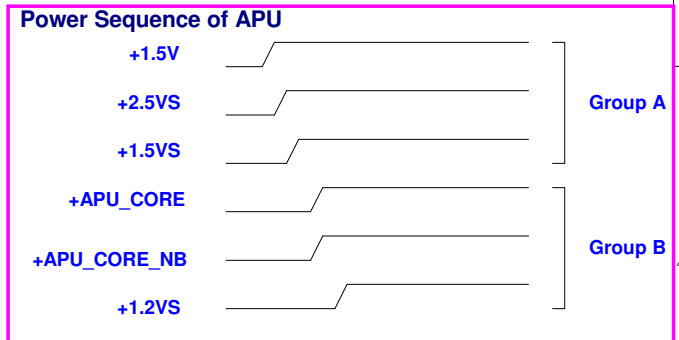
CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	None
	CLKOUT_PCIE1	None
	CLKOUT_PCIE2	10/100 LAN
	CLKOUT_PCIE3	MINI CARD WLAN
	CLKOUT_PCIE4	None
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
	CLKOUT_PEG_B	None

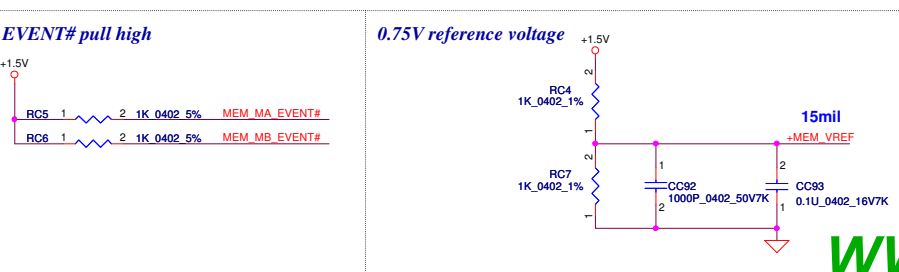
SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



Item	Material P/N	Model DELL PN	Description	Vendor Contact Window
A4-5145M_Dual-Core,FP2(Group B),17W,Richland APU R1_ROH(Production)_HD 8310G	SA00006KC0L	VAW03	S IC A4 SERIES AM5145SHE23HL 2G BGA 813P	AMD
A4-5145M_Dual-Core,FP2(Group B),17W,Richland APU R3_ROH(Production)_HD 8310G	SA00006KC1L	8C6MV	S IC A4 SERIES AM5145SHE23HL 2G BGA 813P A31 I	AMD
A6-5345M_Dual-Core,FP2(Group B),17W,Richland APU R1_ROH(Production)_HD 8410G	SA00006KD0L	VAW03	S IC A6 SERIES AM5345SHE23HL 2.2G BGA 813P	AMD
A6-5345M_Dual-Core,FP2(Group B),17W,Richland APU R3_ROH(Production)_HD 8410G	SA00006KD1L	VGDH2	S IC A6 SERIES AM5345SHE23HL 2.2G BGA 813P A31 I	AMD
A8-5545M_Quad-Core,FP2(Group B),19W,Richland APU R1_ROH(Production)_HD 8510G	SA00006KE0L	VAW03	S IC A8 SERIES AM5545SHE44HL 1.7G BGA 813P	AMD
A8-5545M_Quad-Core,FP2(Group B),19W,Richland APU R3_ROH(Production)_HD 8510G	SA00006KE1L	Y53MJ	S IC A8 SERIES AM5545SHE44HL 1.7G BGA 813P A31 I	AMD
A10-5745M_Quad-Core,FP2(Group B),25W,Richland APU R1_ROH(Production)_HD 8610G	SA00006KH0L	VAW03	S IC A10 SERIES AM5745SIE44HL 2.1G BGA 813P	AMD
A10-5745M_Quad-Core,FP2(Group B),25W,Richland APU R3_ROH(Production)_HD 8610G		缺 DPN		AMD





FP2 DDRIII Memory I/F	Document Number	Rev
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LVDS

HDMI

Route as differential with VSS_SENSE

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Allow_STOP leakage issue

Place near APU

U1D

Place near APU

To LVDS Translator

To HDMI

If not used, pins are left unconnected (DG ref.)
20110111

Asserted as an input to force the processor into the HTC-active state

THERMTRIP shutdown temperature: 125 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

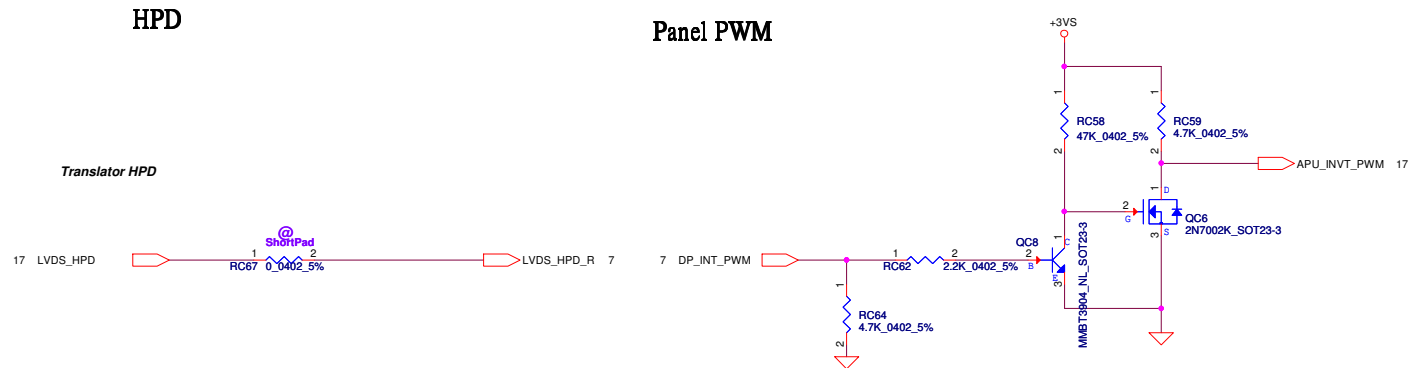
CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

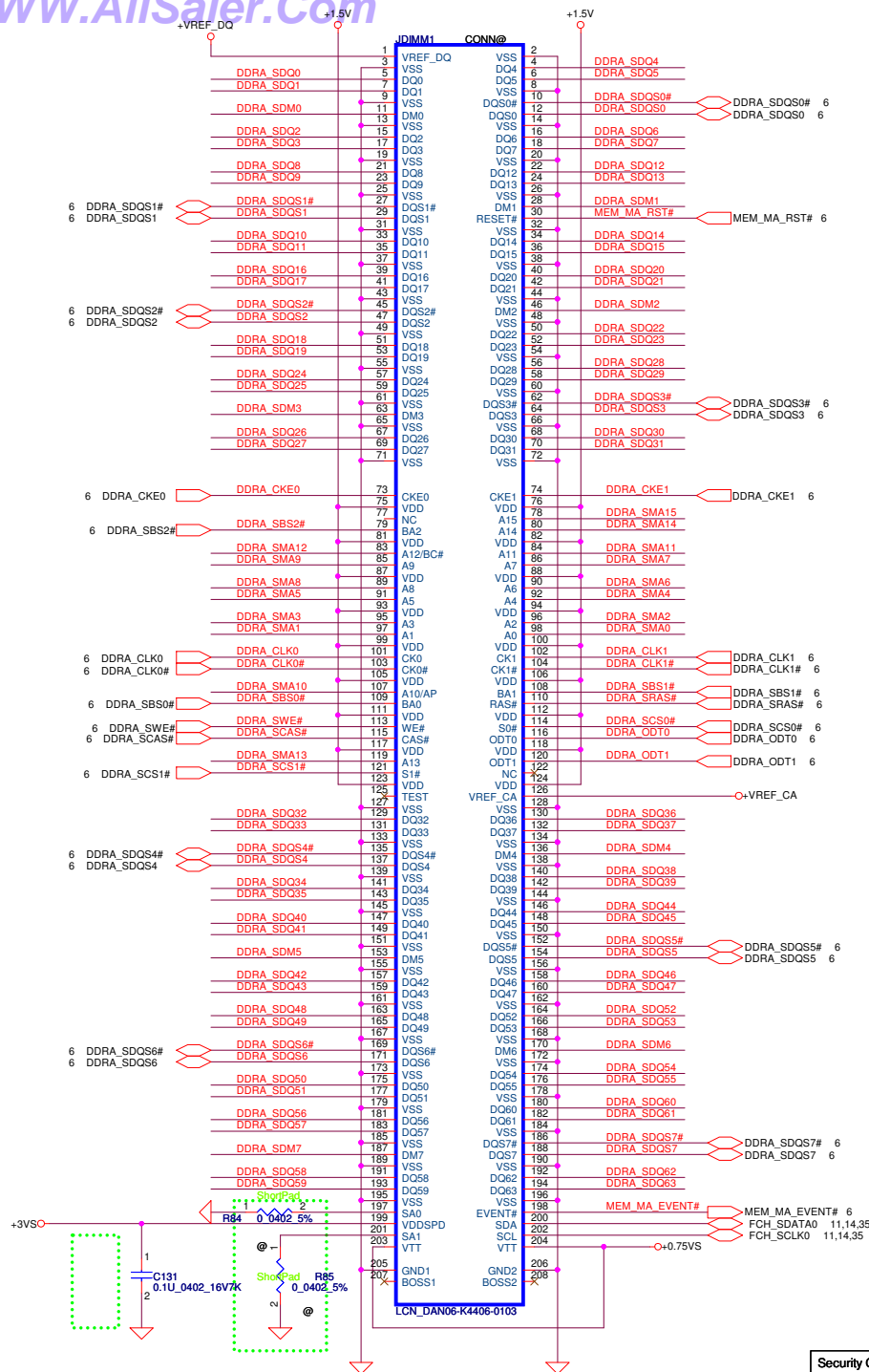
HDT Debug conn

Aux signal are re-configured as I2C signals for DDC. APU AUX pin are 3.3V tolerant
Default follow PANGX setting for pull-high resistor value

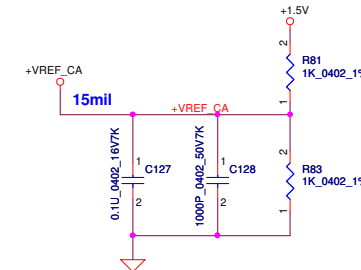
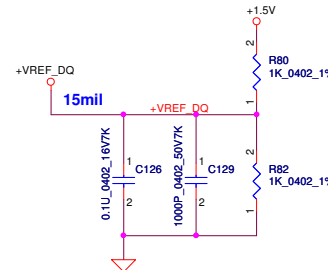
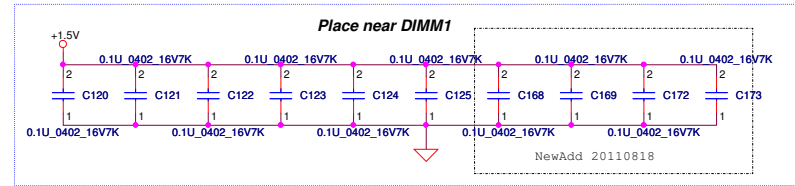
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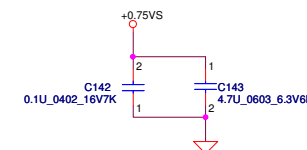
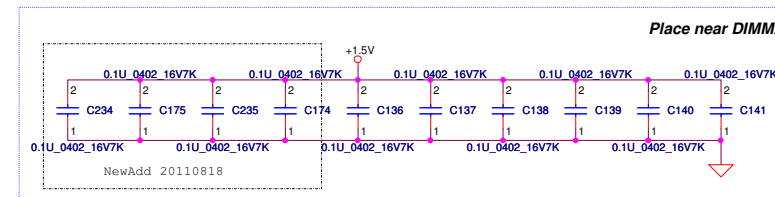
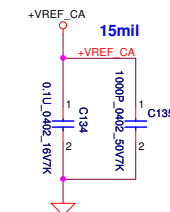
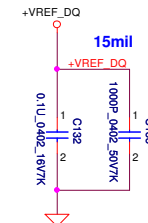
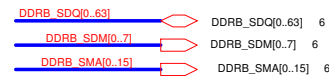
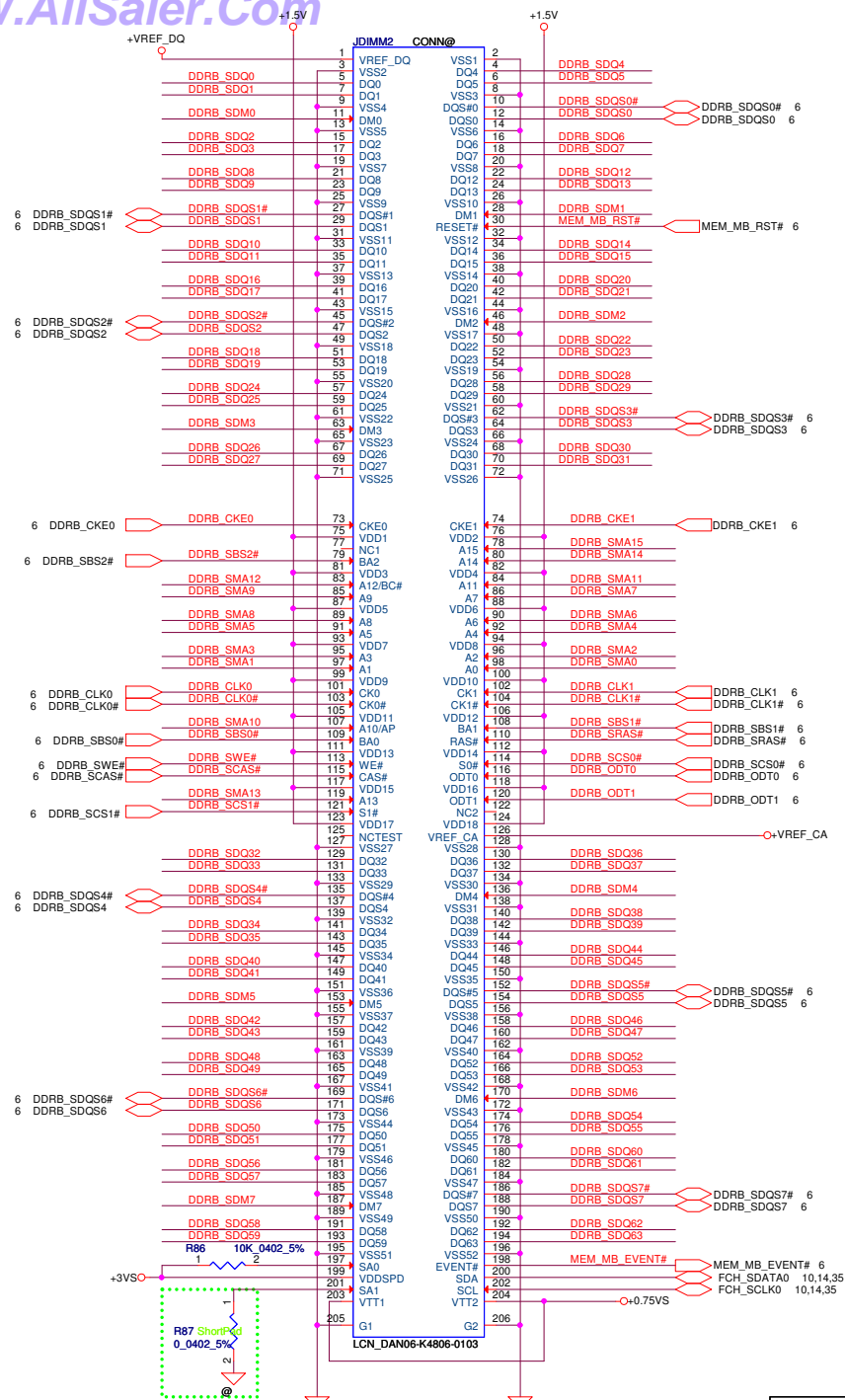
DDRA_SDQ[0..63] 6
DDRA_SDM[0..7] 6
DDRA_SMA[0..15] 6



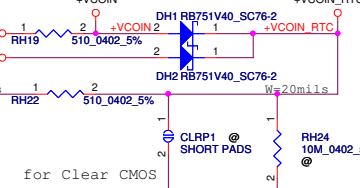
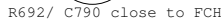
Reverse H:4mm
<Address: 00>

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Reserve H:8mm
<Address: 01>

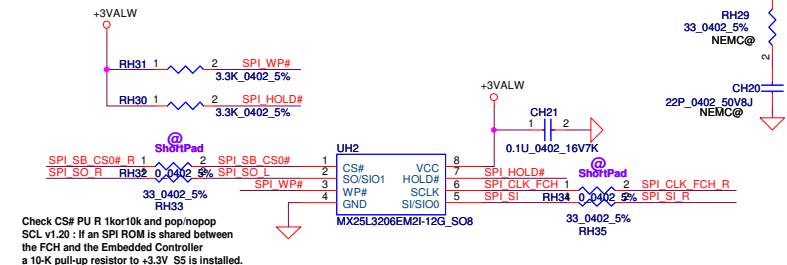
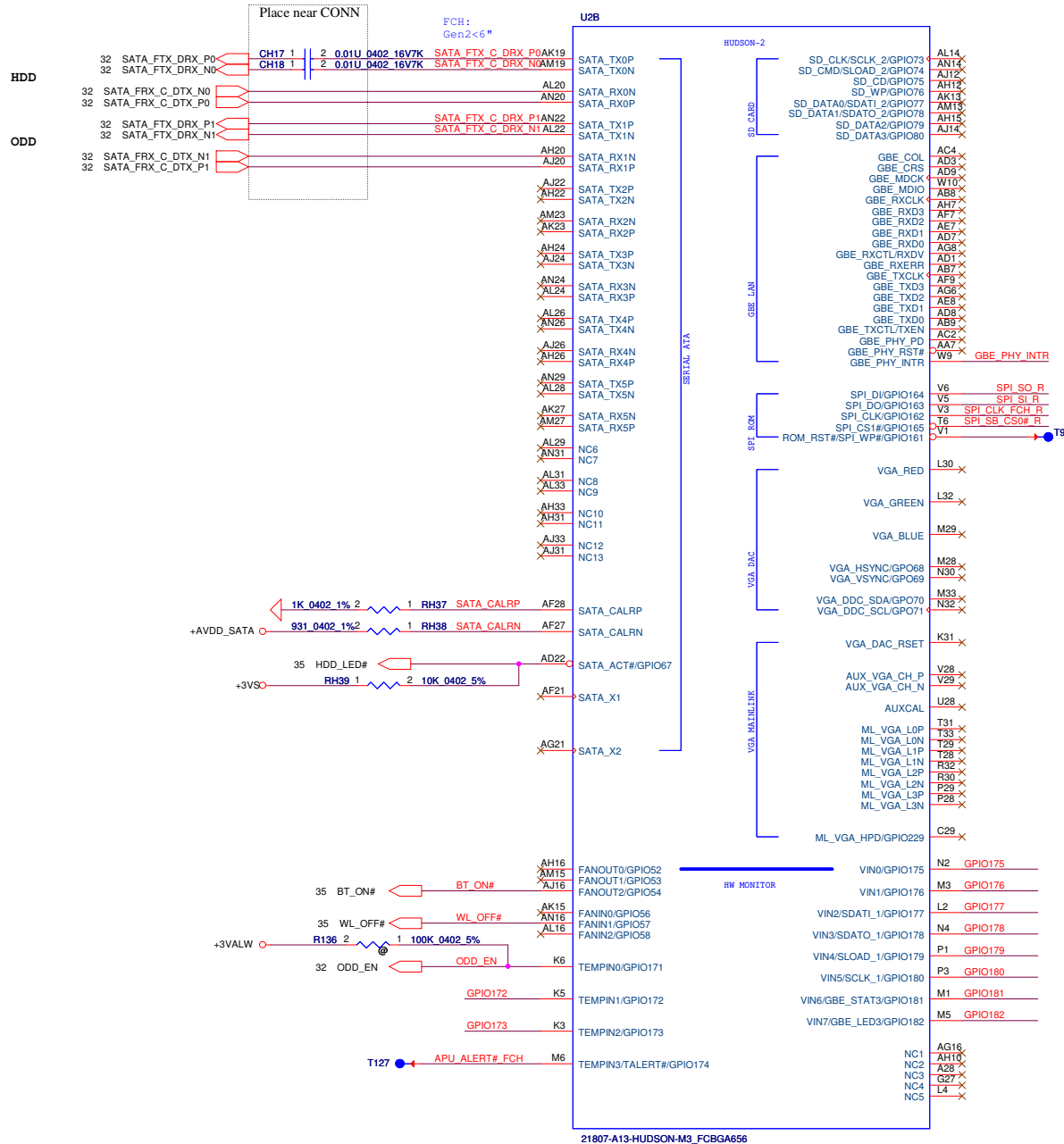


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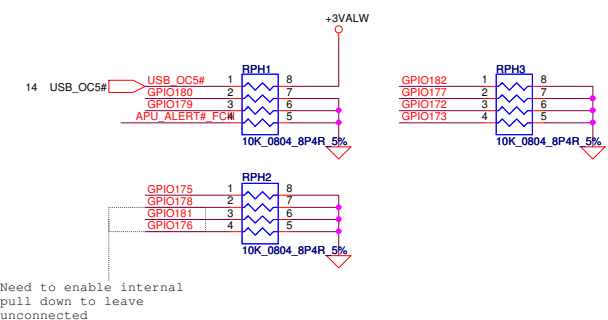
4MB SPI ROM & Non-share ROM.



GBE_PHY_INTR
Pulled-up to +3.3V_S5 with a 10-K 5% resistor.
FCH SCL v1.20 #19-85

GBE_PHY_INTR RH36 1 2 10K 0402 5%

Removed RGMII/MII support and updated termination requirements for GBE_COL, GBE_CRS, GBE_RXERR and GBE_MDIO when RGMII/MII interface is not used.
FCH DGv1.20 / SCL v1.20



Hud@

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21807-A13-HUDSON-M3_FCBGA656				21807-A13-HUDSON-M3_FCBGA656				Rev 1.0			

PCIE_RST2 : Reset PCIE device on Hudson2/3

U20

HUDSON-2

PCIE_RST2#PCI_PME#GEVENT4#

R1#GEVENT22#

SPI_CS3#GMBE_STA1#GEVENT21#

SLP_S3#

SLP_S5#

PWR_BTN#

PWR_GOOD

TEST0

TEST1/TMS

TEST2

GA20IN#GEVENT0#

KB_RST#

LPC_PME#GEVENT3#

LPC_S3#GEVENT23#

LPC_PD#GEVENT5#

SYS_RESET#GEVENT19#

IR_RX1#GEVENT20#

THERMTRIP#SMBALERT#GEVENT2#

WD_PWRGD

RSMRST#

CLK_REQ#SATA_IS0#GPIO64

CLK_REQ#SATA_IS1#GPIO63

SMARTVOL1#SATA_IS2#GPIO60

CLK_REQ#SATA_IS3#GPIO60

SATA_IS4#FANOUT3#GPIO55

SATA_IS5#FANIN3#GPIO59

SPKR#GPIO66

SCL0#GPIO43

SDA0#GPIO47

SCL1#GPIO227

SDA1#GPIO228

CLK_REQ#FANIN4#GPIO62

CLK_REQ#FANOUT4#GPIO61

IR_LED#L1#GPIO184

SMARTVOL2#SHUTDOWN#GPIO51

DDR3_RST#GEVENT7#VGA_PD

GBE_LED0#GPIO183

SPI_HOLD#GBE_LED1#GEVENT9#

GBE_LED2#GEVENT10#

GBE_STAT0#GEVENT11#

CLK_REQ#GPIO65#OSCIN#IDLEEXT#

BLINK#USB_OC7#GEVENT18#

USB_OC8#IR_TX1#GEVENT6#

USB_OC9#IR_TX0#GEVENT17#

USB_OC4#IR_RX0#GEVENT18#

USB_OC3#AC_PRE#TDO#GEVENT15#

USB_OC2#TCK#GEVENT14#

USB_OC1#TDO#GEVENT13#

USB_OC0#SPI_TPM_CS#TRST#GEVENT12#

AZ_BITCLK

AZ_SDOUT

AZ_SDOIN#GPIO167

AZ_SDOIN#GPIO168

AZ_SDOIN#GPIO169

AZ_SDOIN#GPIO170

AZ_SYNC

AZ_RST#

P22_DAT#SDA4#GPIO187

P22_CLK#SCL4#GPIO188

SPI_CS2#GBE_STA2#GPIO166

P22KB_DAT#GPIO189

P22KB_CLK#GPIO190

P22M_CLK#GPIO191

P22M_CLK#GPIO192

KSO_0#GPIO209

KSO_1#GPIO210

KSO_2#GPIO211

KSO_3#GPIO212

KSO_4#GPIO213

KSO_5#GPIO214

KSO_6#GPIO215

KSO_7#GPIO216

KSO_8#GPIO217

KSO_9#GPIO218

KSO_10#GPIO219

KSO_11#GPIO220

KSO_12#GPIO221

KSO_13#GPIO222

KSO_14#GPIO223

KSO_15#GPIO224

KSO_16#GPIO225

KSO_17#GPIO226

KSI_0#GPIO201

KSI_1#GPIO202

KSI_2#GPIO203

KSI_3#GPIO204

KSI_4#GPIO205

KSI_5#GPIO206

KSI_6#GPIO207

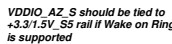
KSI_7#GPIO208


21807-A13-HUDSON-M3_FCBGA656

Hud@

Board Config.	GPIO189	GPIO190	Function
	0	0	DIS-PX4
	0	1	Reserved
	1	0	DIS-PURE
	1	1	UMA

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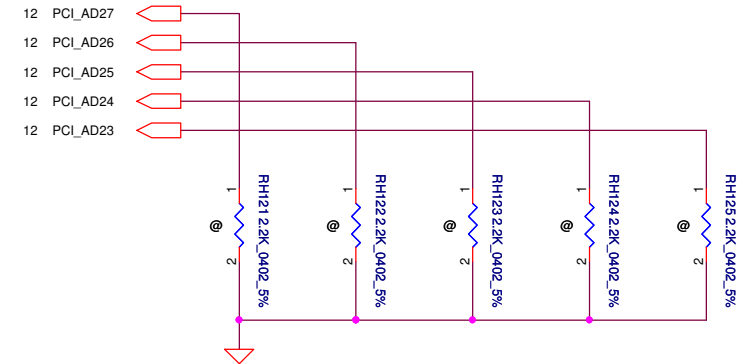
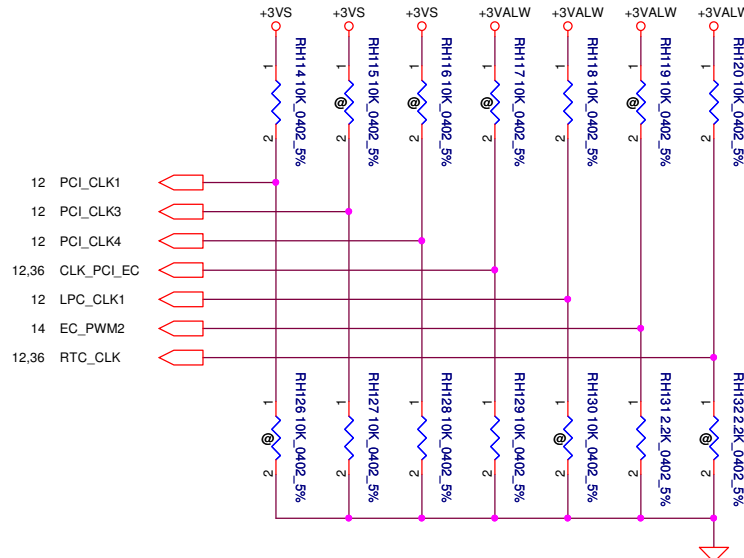
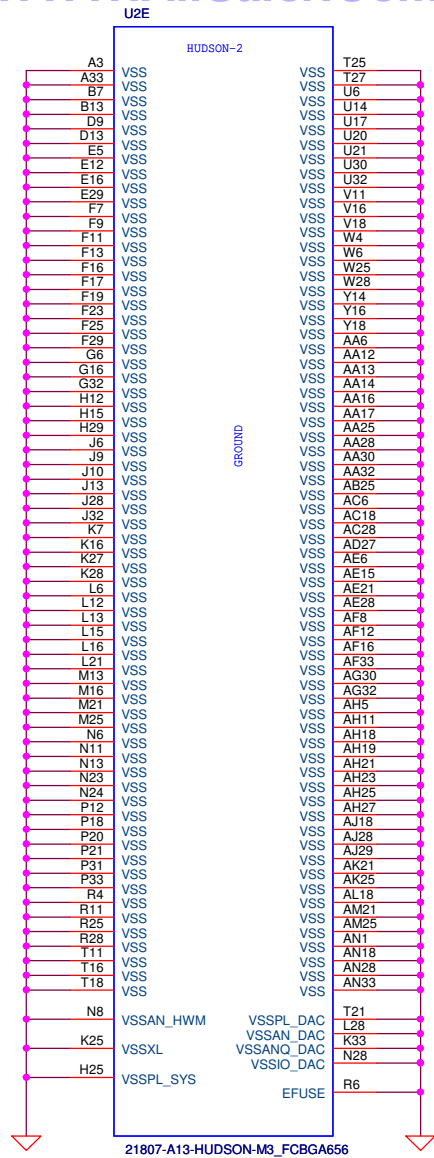
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

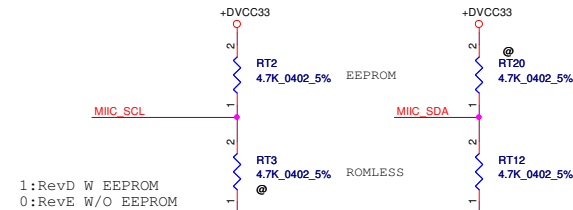
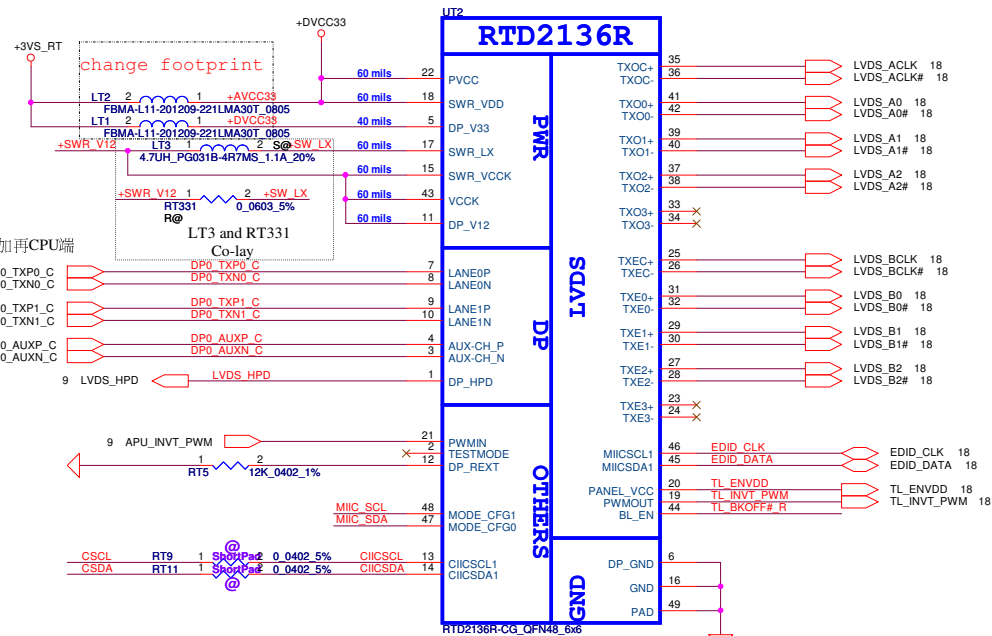
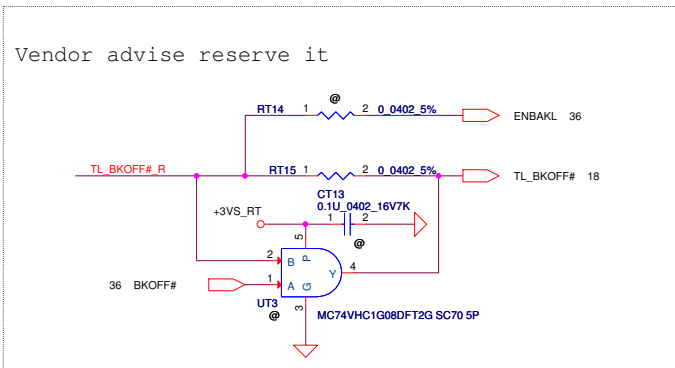
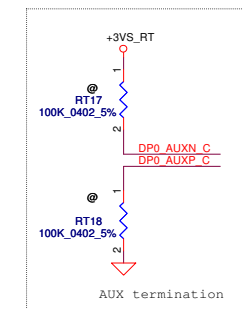
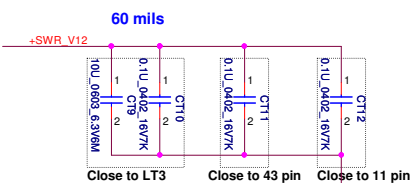
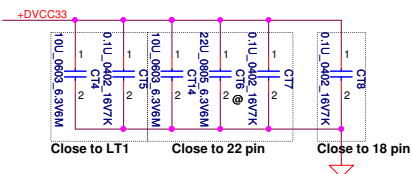
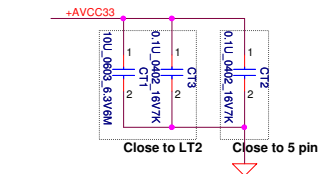
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



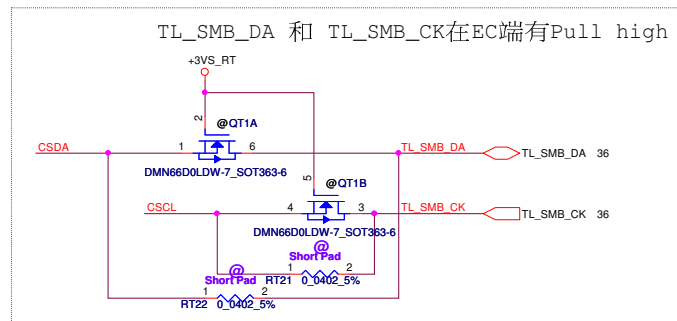
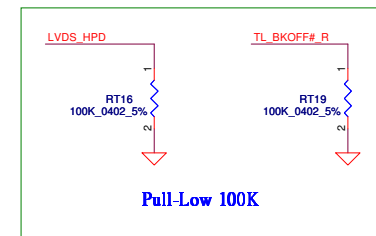
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				Date:	Wednesday, July 10, 2013	Sheet 16 of 52

Power Consumption:

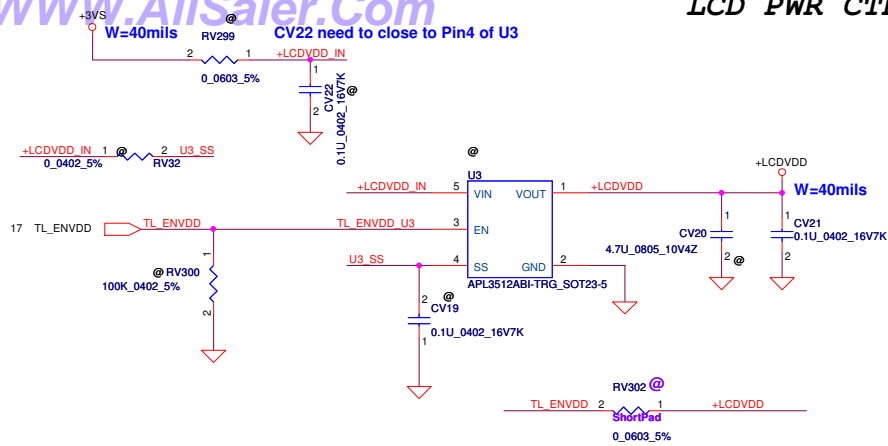
Pin22 (DPV33) < 20mA
 Pin 11 (DP_V12) < 100mA
 Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
 Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
 Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
 Pin 22 (PVCC) < 50 mA
 Pin 43 (VCCK) < 50mA



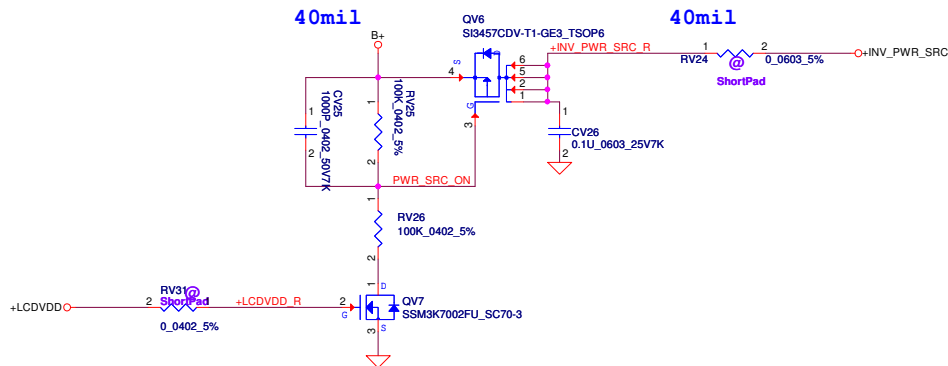
		Pin47 MIIC_SDA	
		0	1
Pin48 MIIC_SCL	0	x	EP MODE
	1	ROM	EEPROM



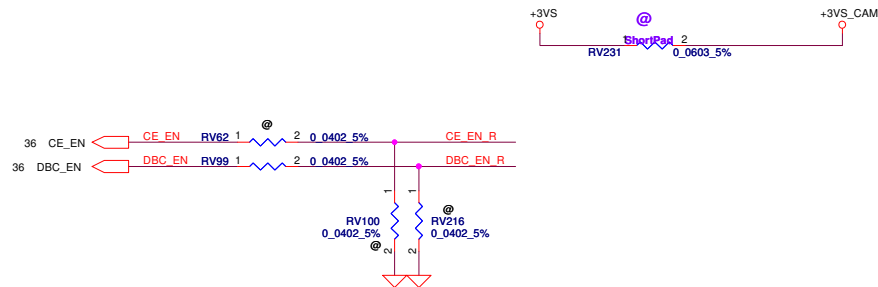
LCD PWR CTRL



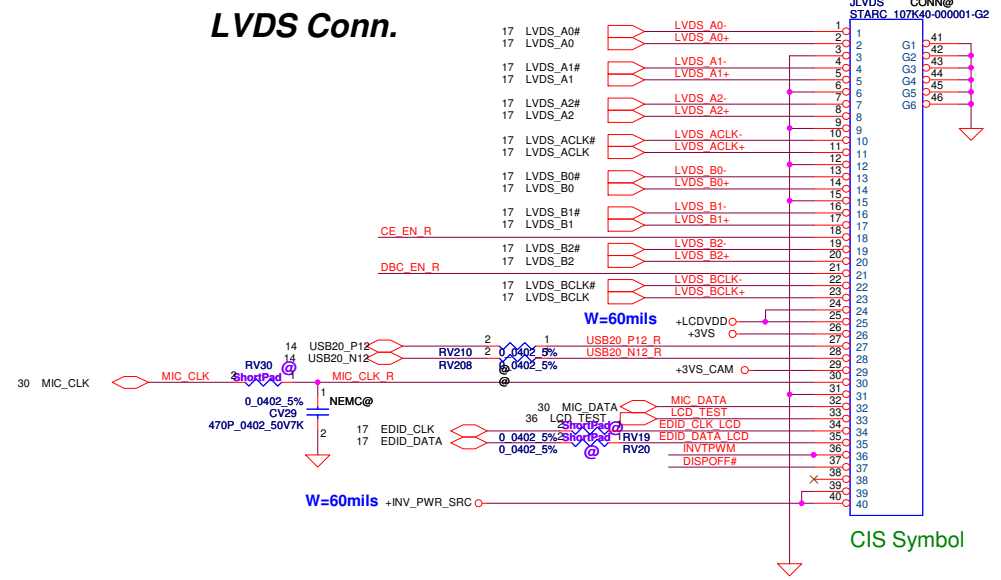
LCD backlight PWR CTRL



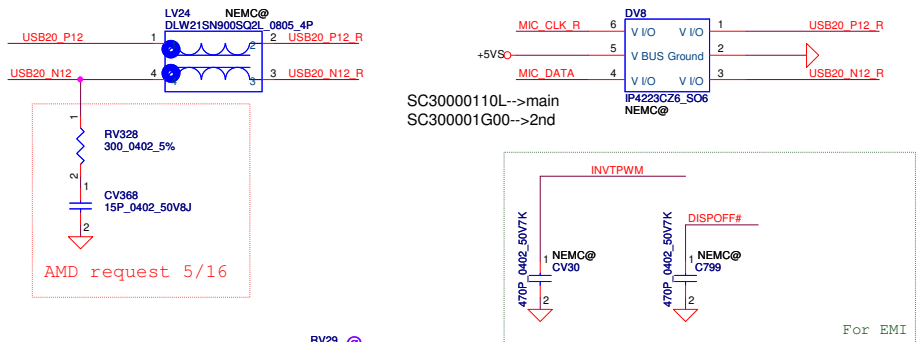
Wedcam PWR CTRL



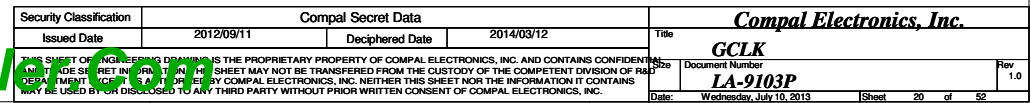
LVDS Conn.



* Reserved for EMI/ESD/RF need to close to JLVDS



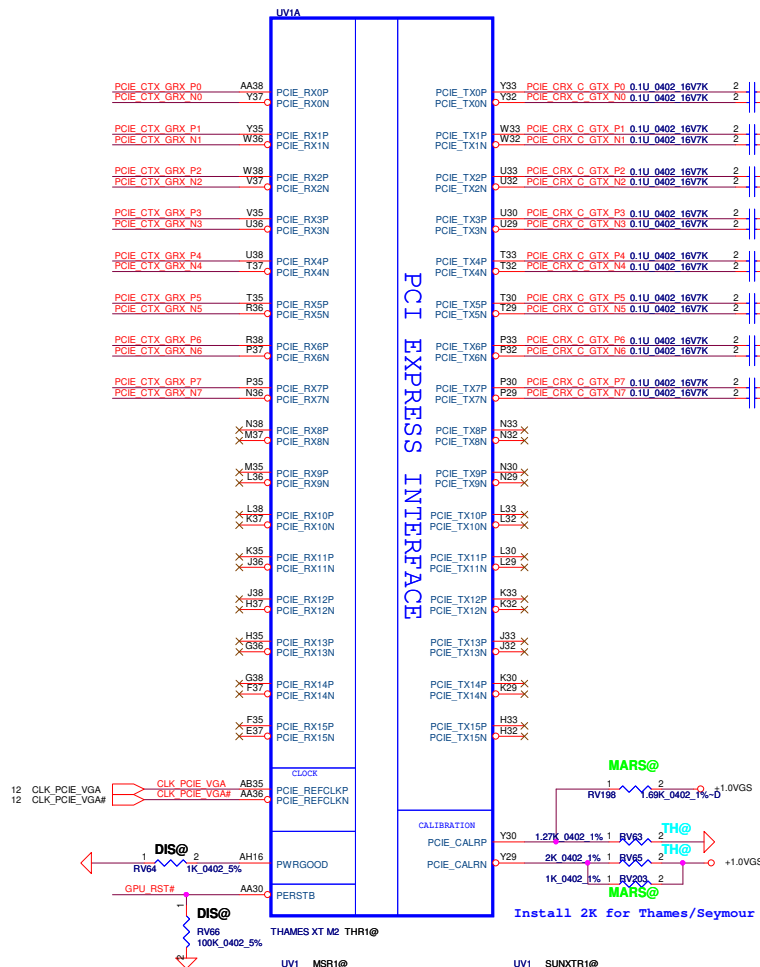
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				LA-9103P	
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5 PCIE_CTX_GRX_P[7..0] PCIE_CTX_GRX_P[7..0]
5 PCIE_CTX_GRX_N[7..0] PCIE_CTX_GRX_N[7..0]

GFX PCIE LANE REVERSAL

PCIE_CRX_GTX_P[7..0] PCIE_CRX_GTX_P[7..0] 5
PCIE_CRX_GTX_N[7..0] PCIE_CRX_GTX_N[7..0] 5

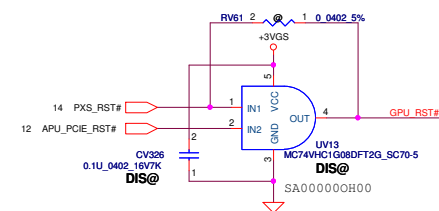
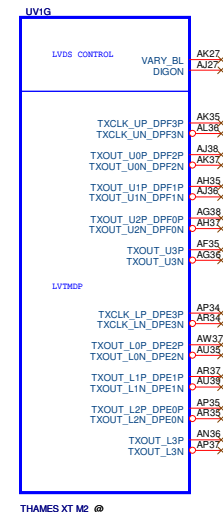


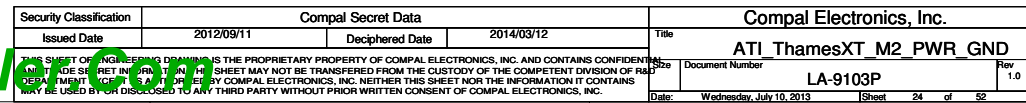
UV1 MSR1@
SA00005X10L
MARS-PRO_FCBGA962-D
MARS FFC

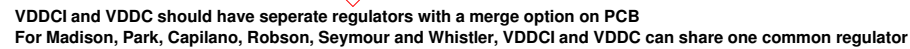
UV1 SUNXTR1@
SA00006G60L
SUN XT M2_FCBGA962

UV1 SUNXTR3@
SA00006G61L
SUN XT M2_FCBGA962

LVDS Interface



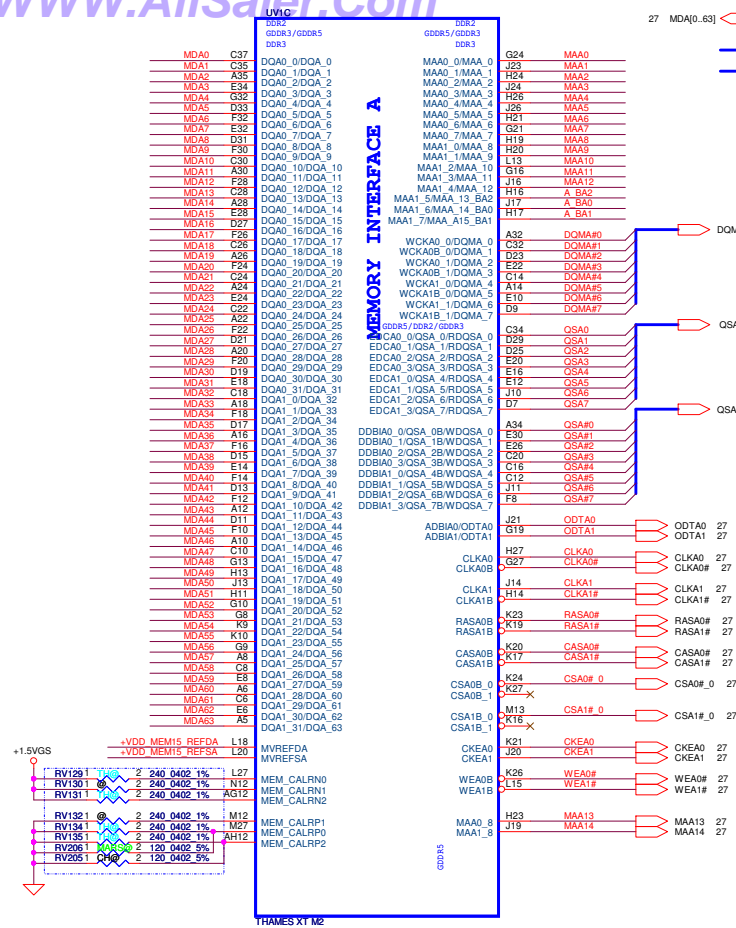




For MARS/VENUS/HEATHROW/CHELSEA
BIF_VDDC should be connected with 0.95V

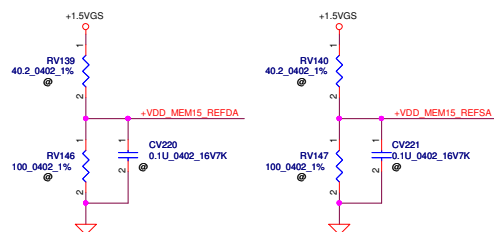
On Heathrow/Chelsea/Venus/Mars only
PCIE VDDC : 0.95V @ 1.3A (GEN3.0)

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				2014/03/12	
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				ATI ThamesXT M2 Power	
Size				Document Number	
				LA-9103P	
Date				Wednesday, July 10, 2013	
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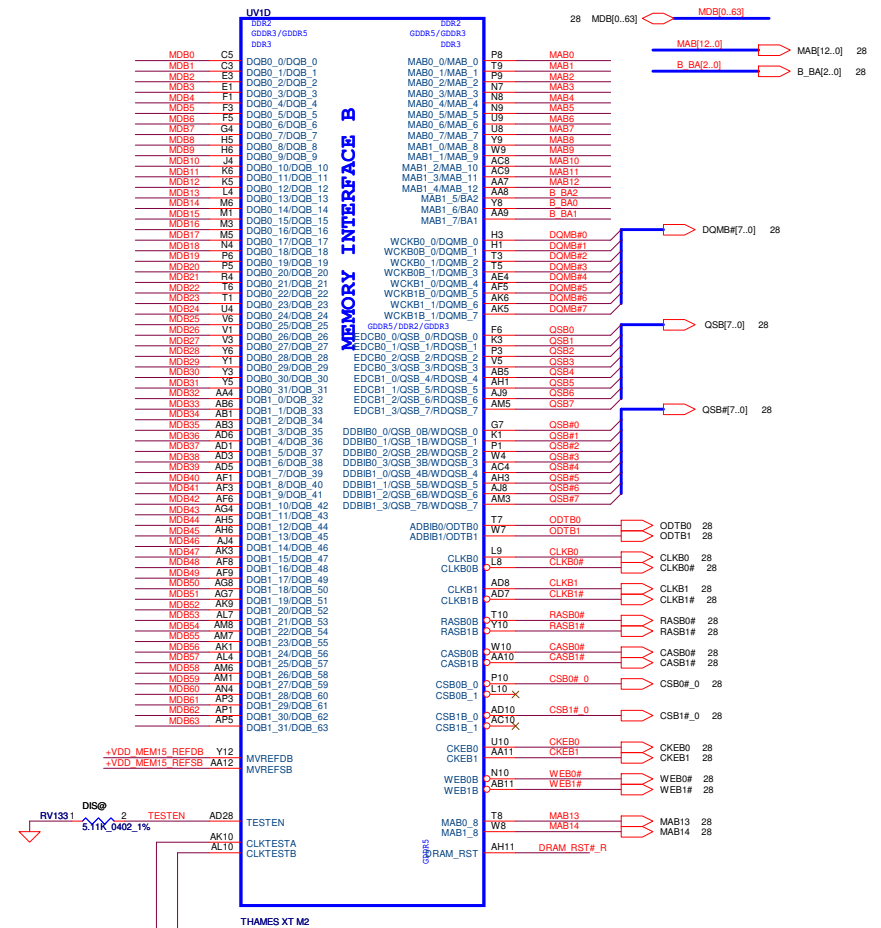
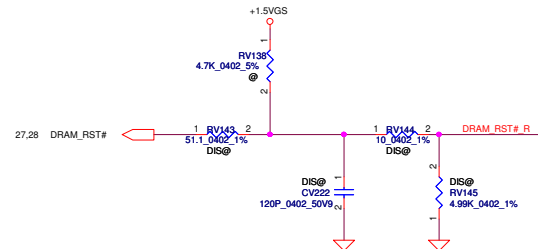
Co-lay Thames/Mars Pro/Chelsea

	Thames M2	Mars Pro	Chelsea M2
RV129	POP	@	@
RV130	@	@	@
RV131	POP	@	@
RV132	@	@	@
RV134	POP	@	@
RV135	POP	@	@
RV206	@	MARS@	@
RV205	@	@	POP

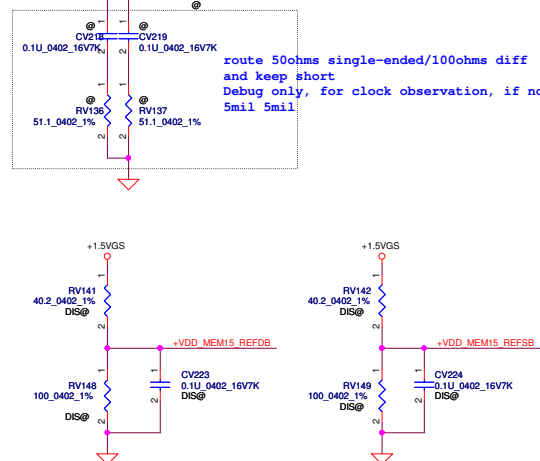


This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and |C| Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

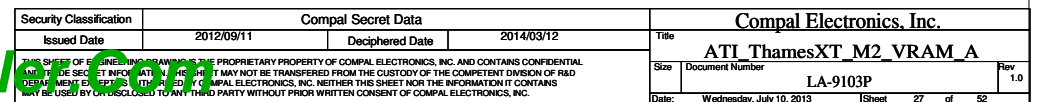
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



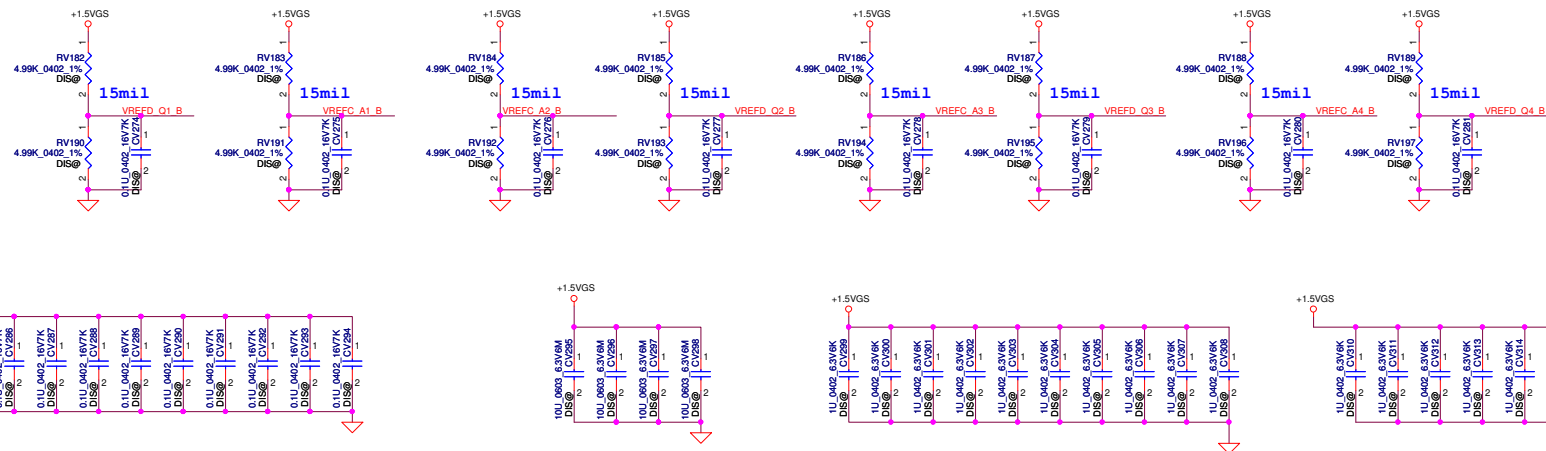
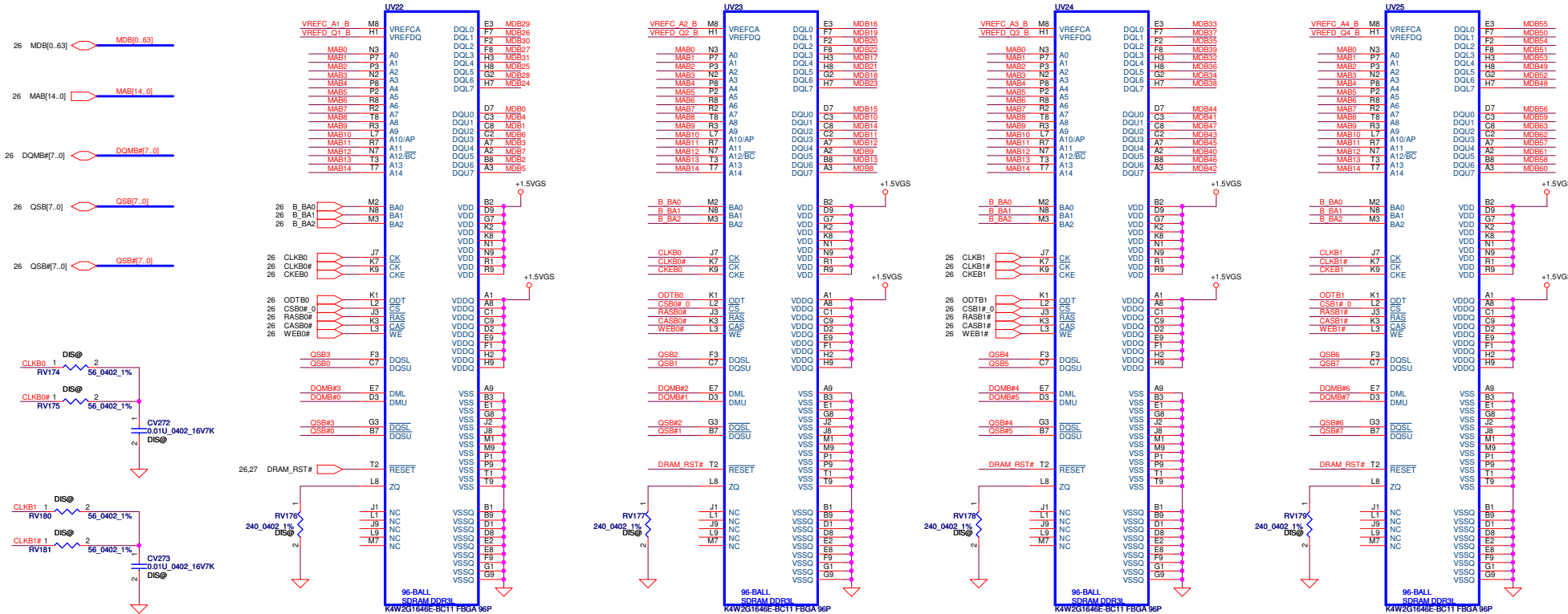
```
route 50ohms single-ended/100ohms diff
and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil
```



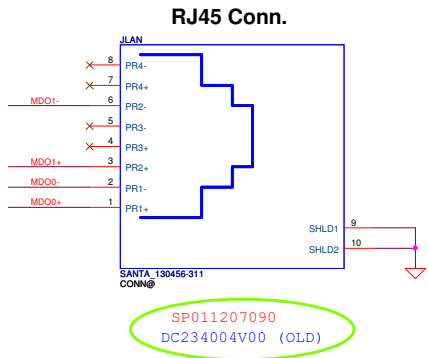
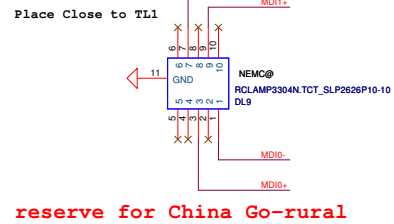
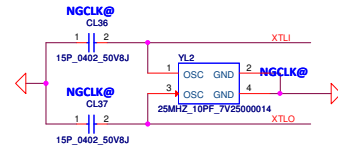
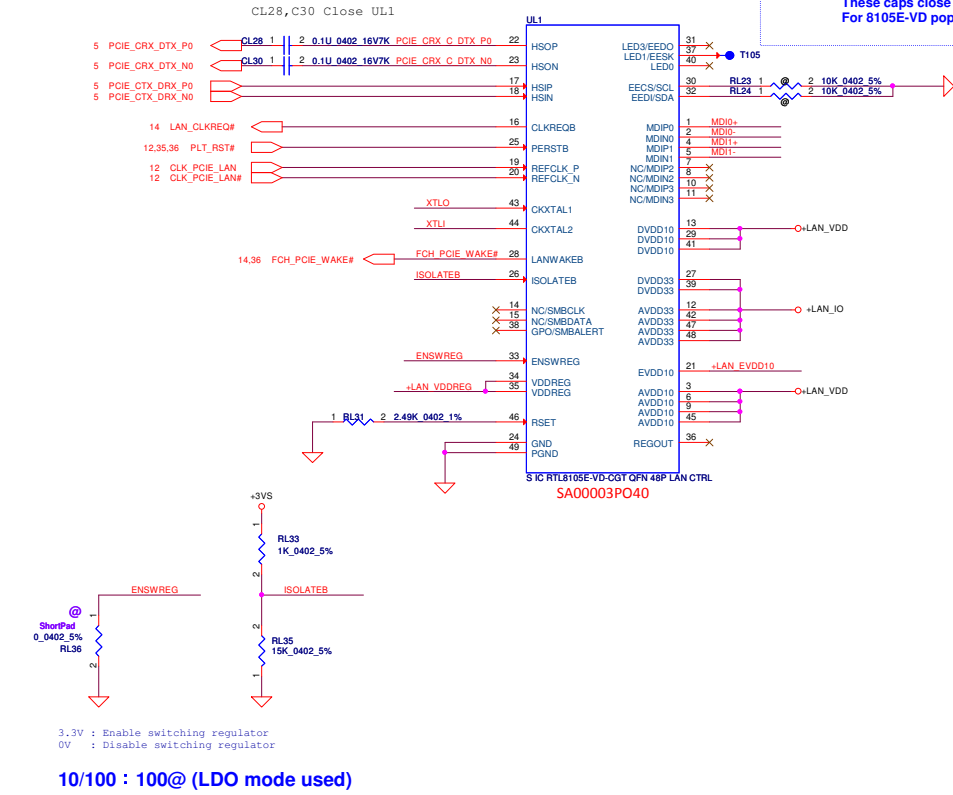
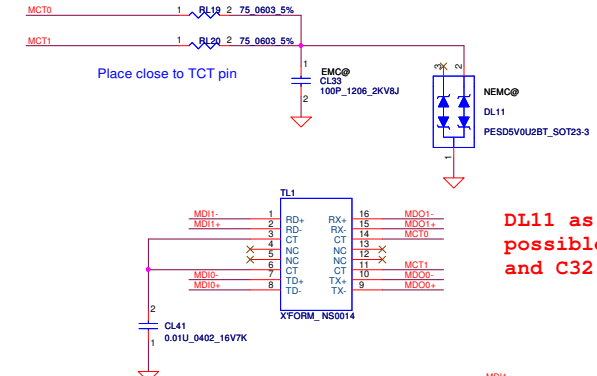
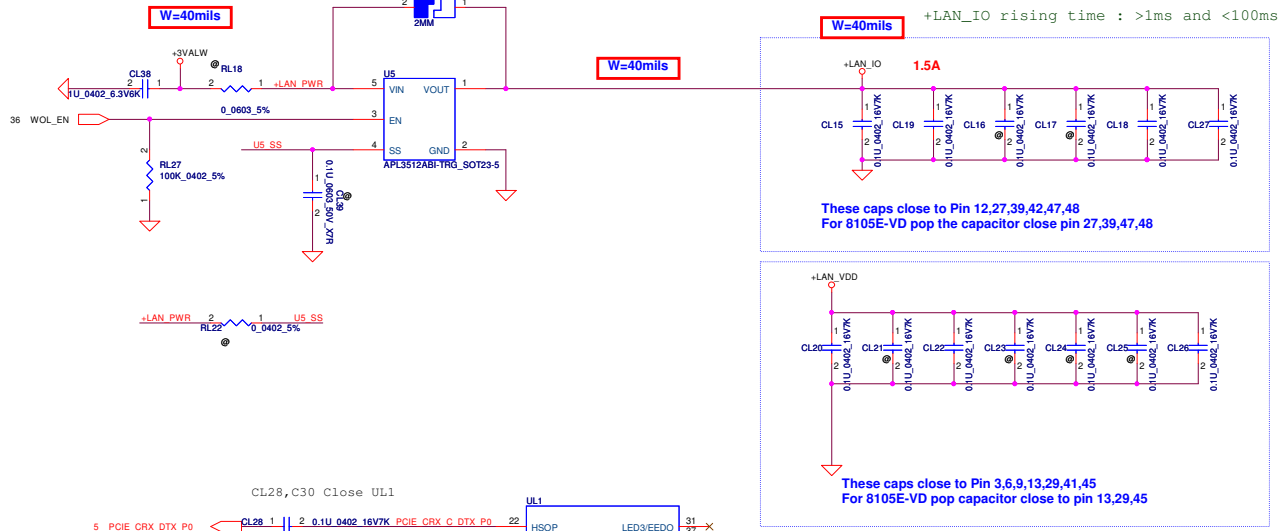
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	ATI ThamesXT_M2_MEM IF	
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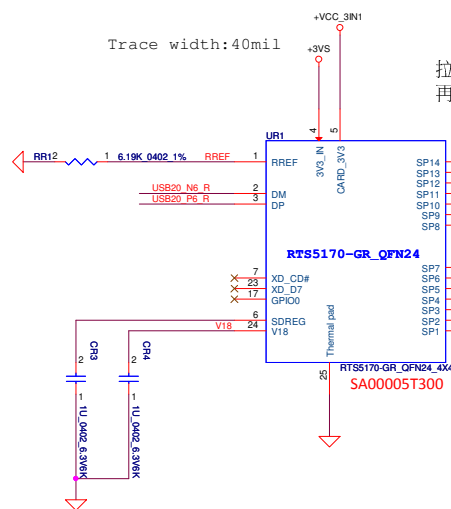
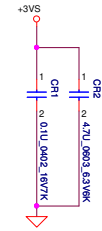
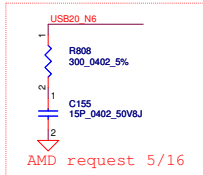
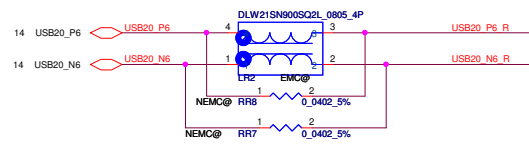
CHANNEL B: 256MB/512MB DDR3



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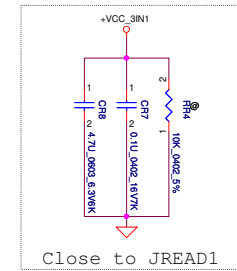
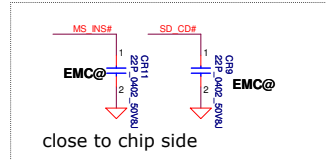
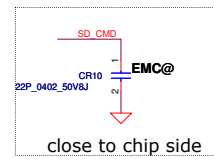
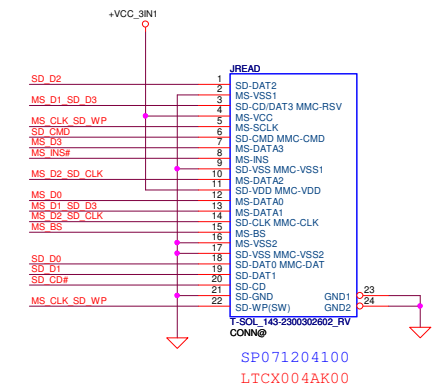
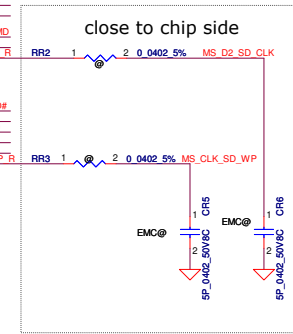


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拉MS_D2_SD_CLK到Conn pin 14 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 22 SD_W



[illegible]

RX

13 SATE_FRX_C_DTX_N1
13 SATE_FRX_C_DTX_P1

14,36 ODD_DA#

RNS 1 0.0402 5%
RN13 2 0.0402 5%
RN14 2 0.0402 5%

5V5_ODD

JBTB1

1 2
3 4
5 6
7 8
9 10
11 12

13 GND
14 GND
15 GND

E-T_1133-012C-01R

16 GND
17 GND
18 GND

TX

1 SATE_FTX_DRX_P1_C
1 SATE_FTX_DRX_N1_C

ODD_DETECT#

RH43 2 0.0402 5%
RH42 2 0.0402 5%

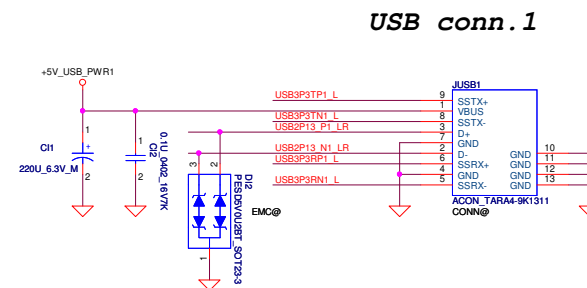
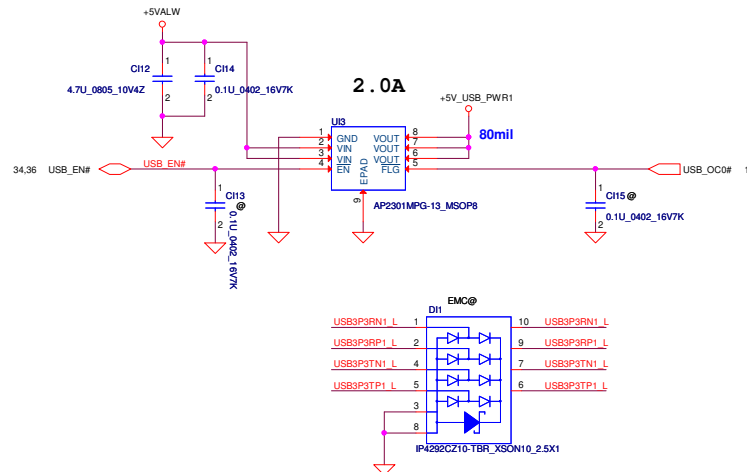
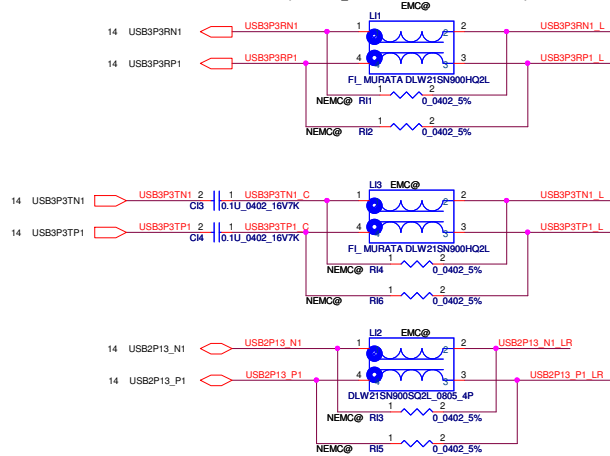
14 ODD_DETECT#

SP02000MJ00
SP02000G800 (OLD)

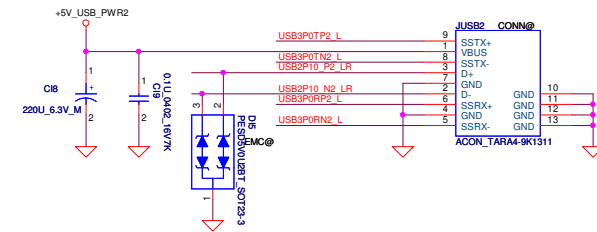
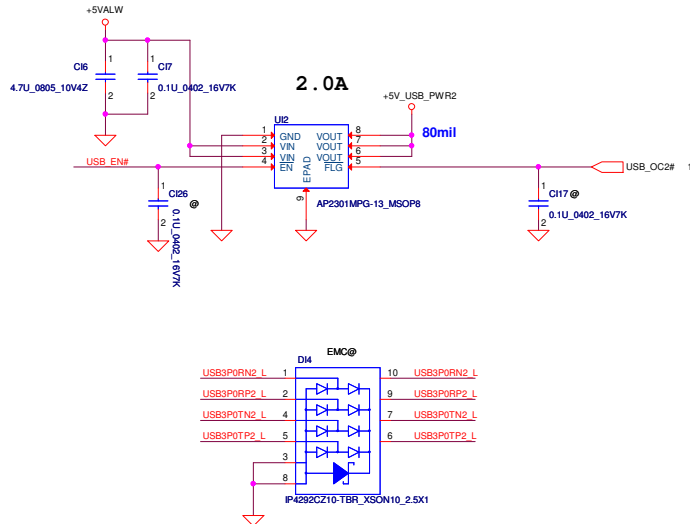
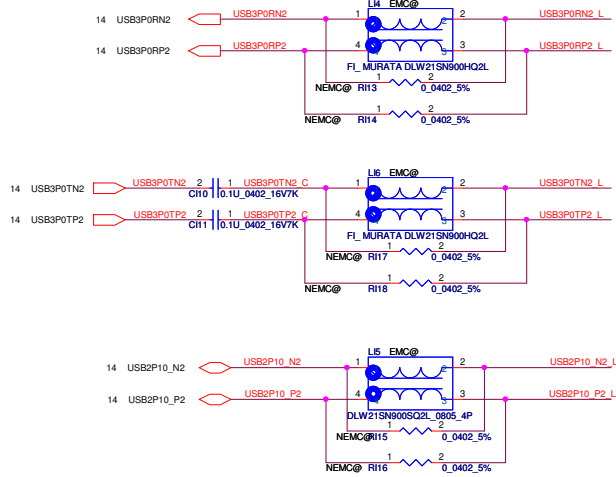
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WWW.AliSale.com

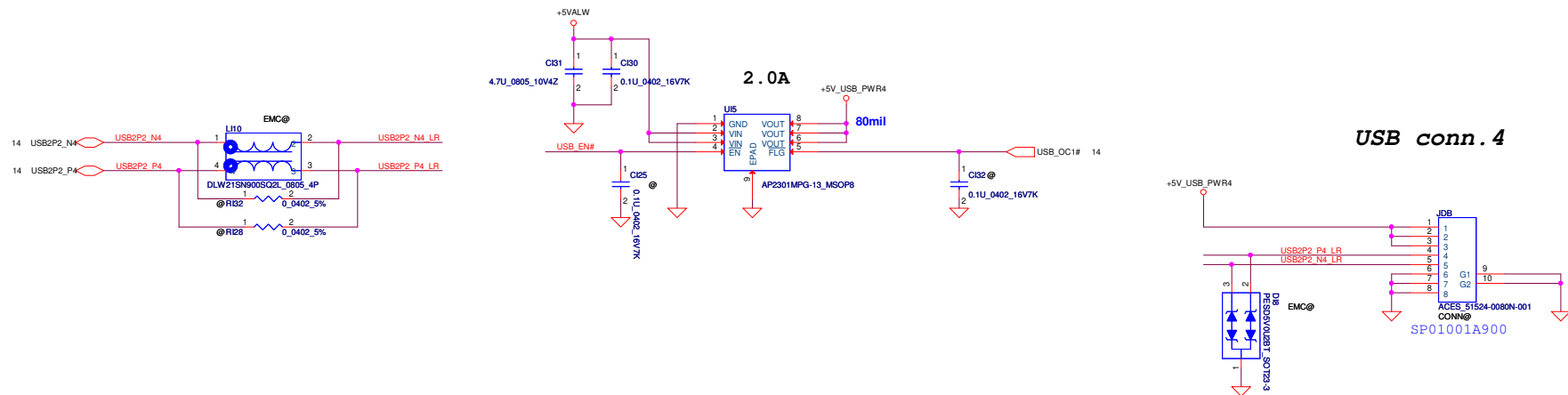
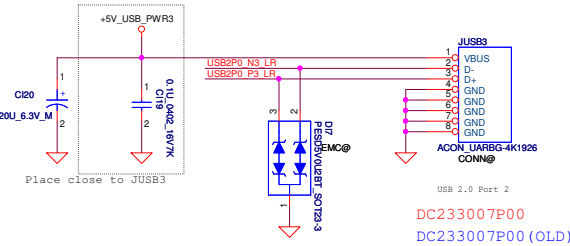
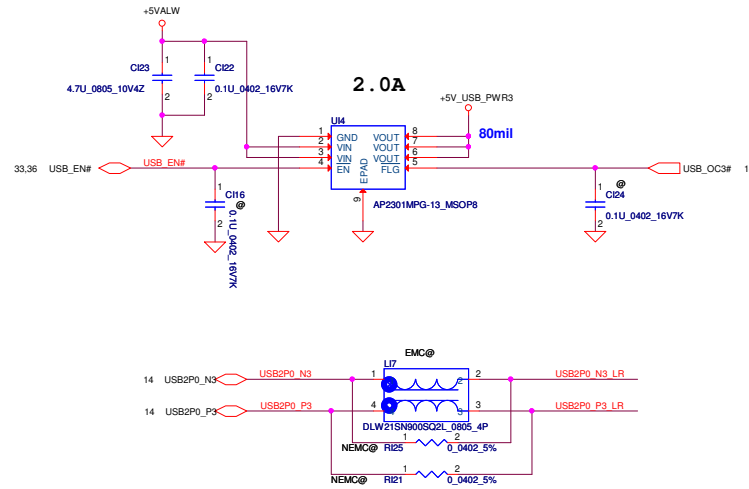
9/20 QAK Intel USB3.0 issue
Change LI1, LI3, LI4, LI6 Part
PN: from SM070000S80 (S COM FL_MURATA DLW21SN900SQ2L 0805)
To SM070000S80 (S COM FL_CHENG HANN WCM2012F2SF-670T04)
1/22 Change LI1, LI3, LI4, LI6 Part
PN: from SM070000S80 (S COM FL_CHENG HANN WCM2012F2SF-670T04)
To SM070001E00 (S COM FL_MURATA DLW21SN900HQ2L)~Main
To SM070001S00 (S COM FL_KINGCORE WCM-2012HS-900T)~2nd



USB conn.1

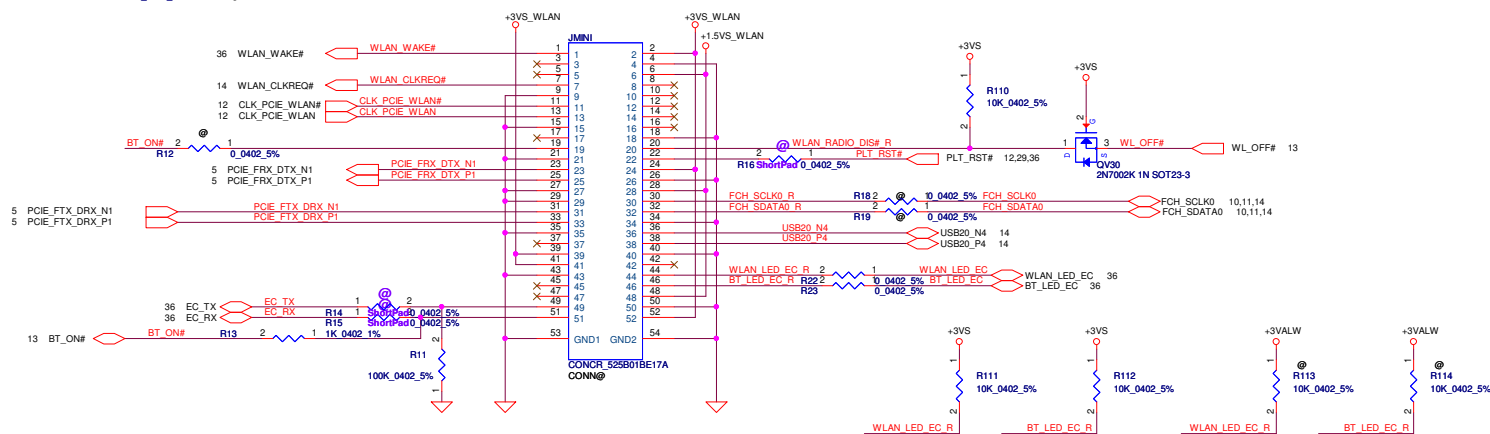


USB conn.2

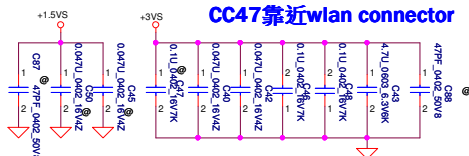


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Mini WLAN/WIMAX H=6.7

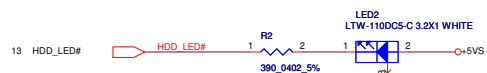


CC47靠近wlan connector

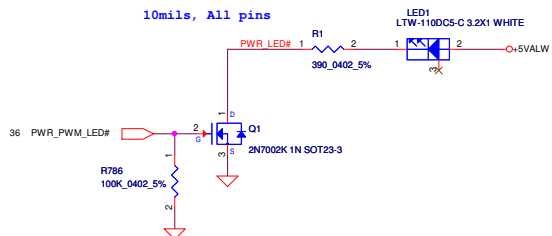


R111, R112
Please Close to JMINI

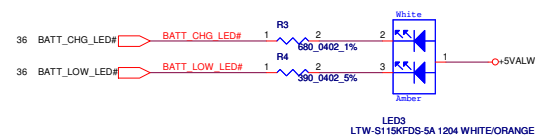
HDD LED



Power LED

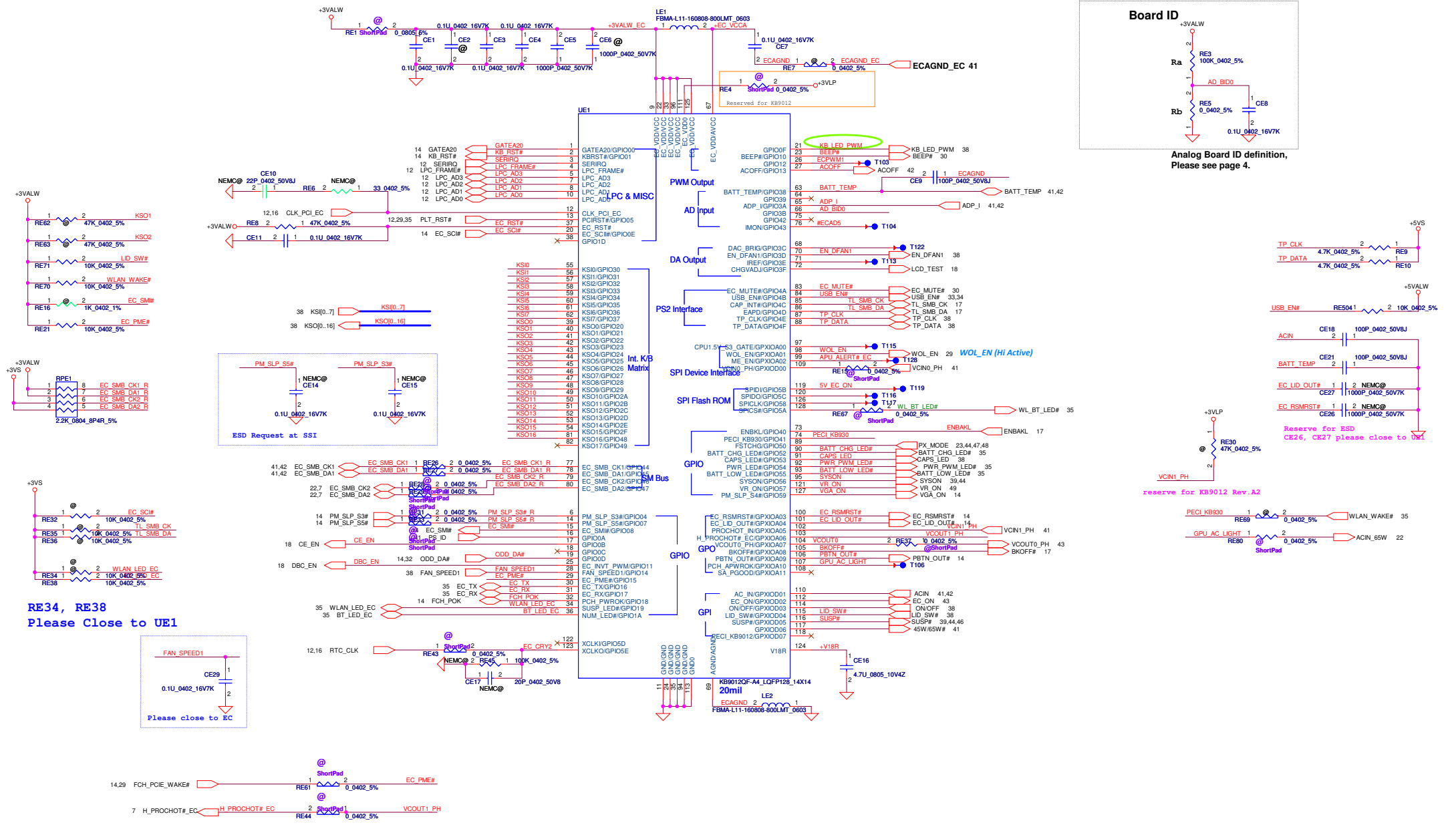


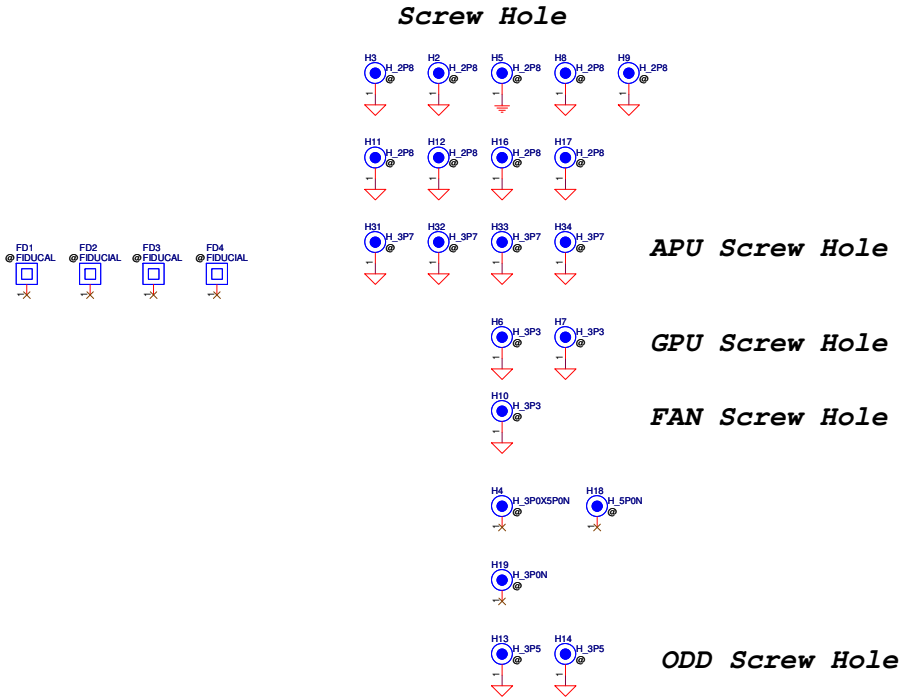
Battery LED



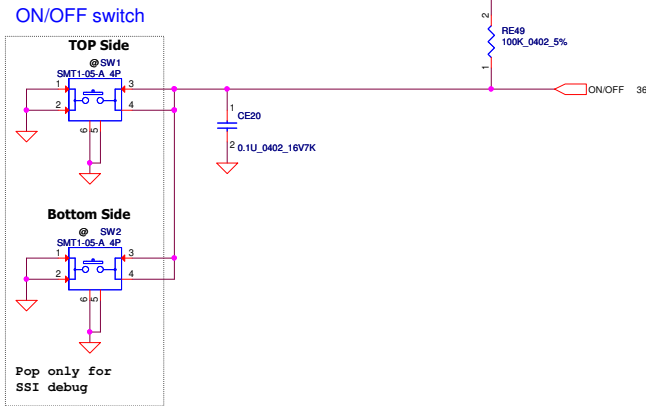
Wireless LED



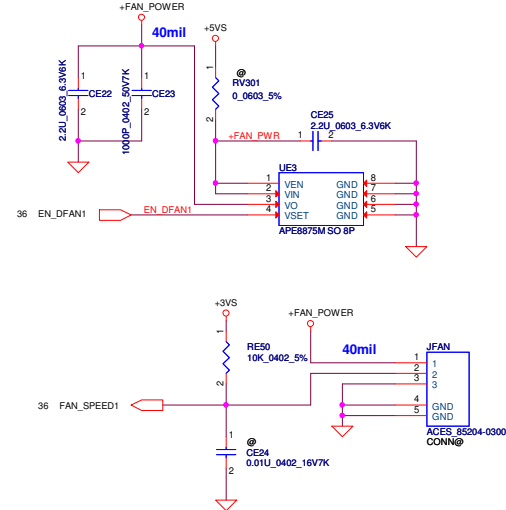




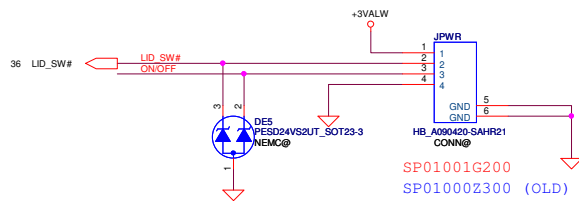
Power ON Circuit



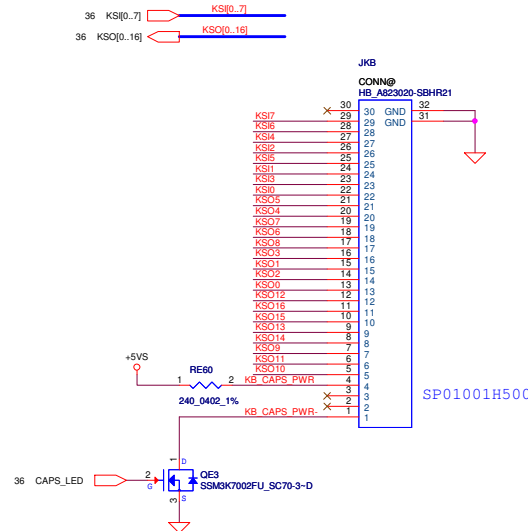
FAN Control circuit



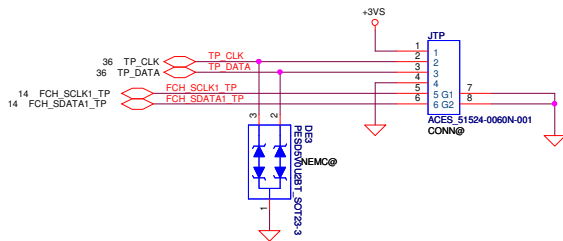
POWER/B



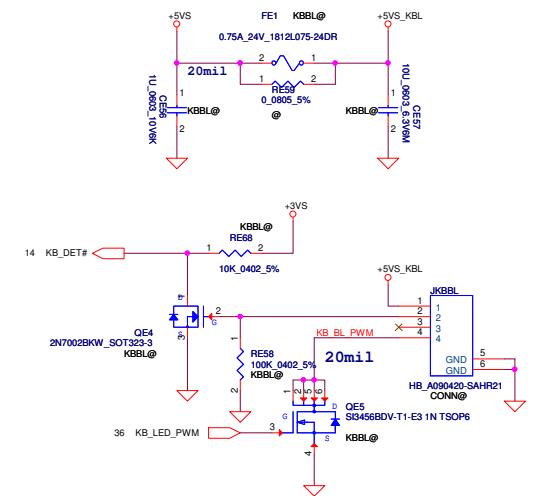
INT_KBD Conn.



Touch pad

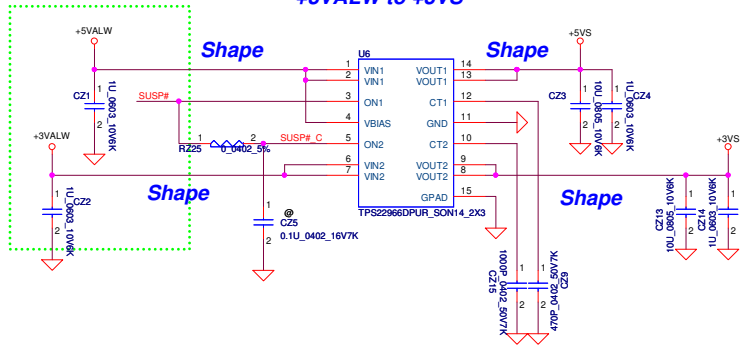


* Key Board Back Light

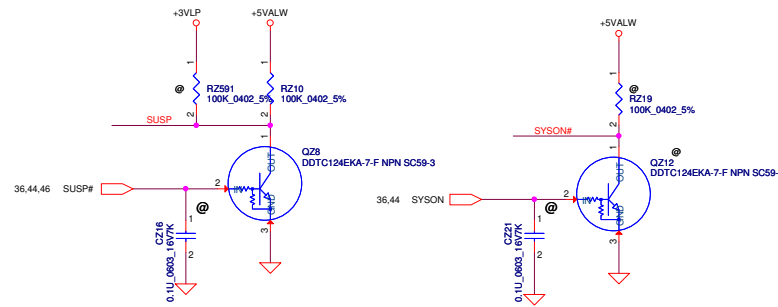
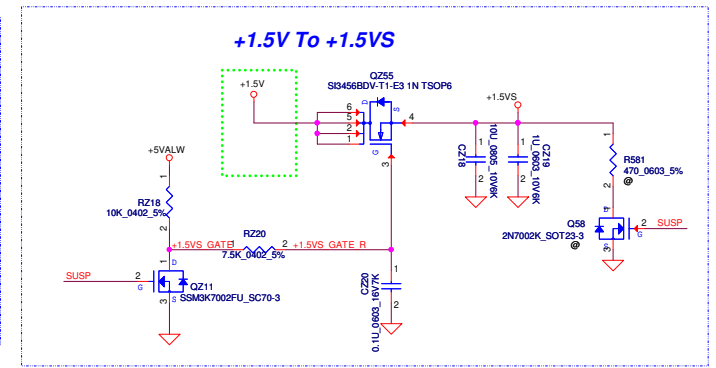
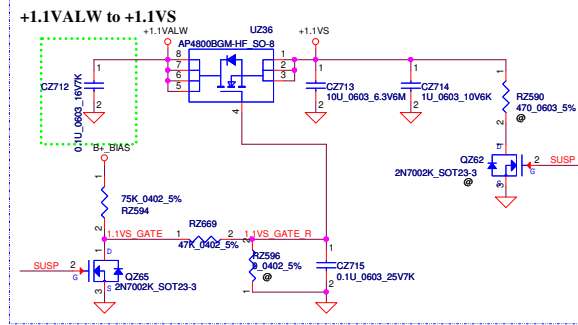


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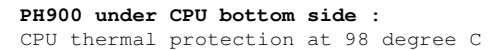
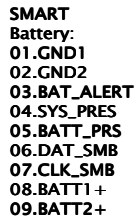
+5VALW to +5VS
+3VALW to +3VS



CTx (pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835



[illegible][illegible]



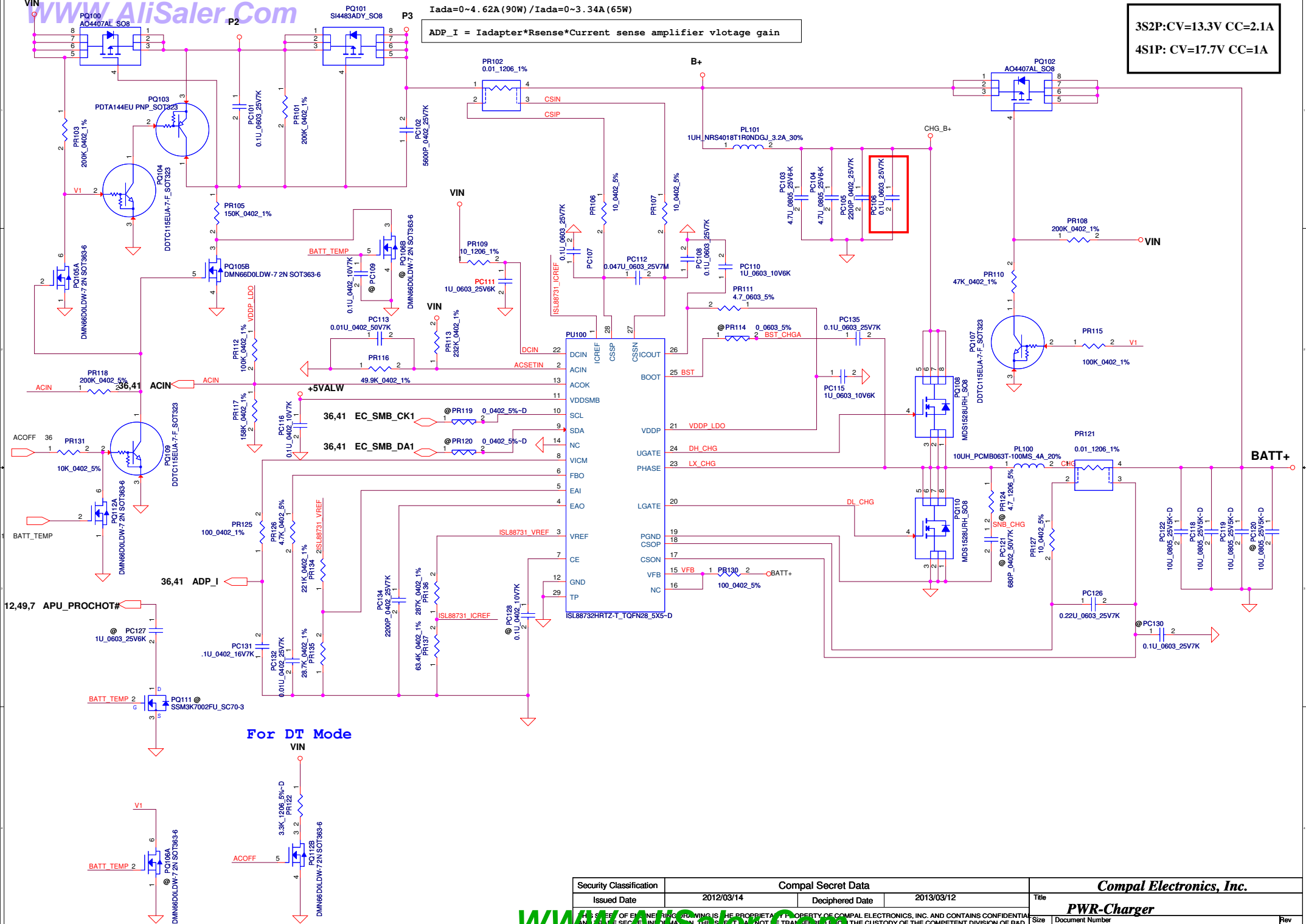
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$I_{ada}=0\sim 4.62A(90W) / I_{ada}=0\sim 3.34A(65W)$

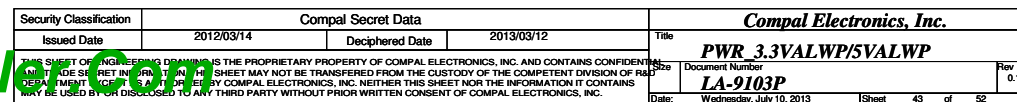
$$ADP_I = I_{\text{adapter}} \cdot R_{\text{sense}} \cdot \text{Current sense amplifier voltage gain}$$

3S2P:CV=13.3V CC=2.1A

4S1P: CV=17.7V CC=1A



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				Size	Document Number	Rev
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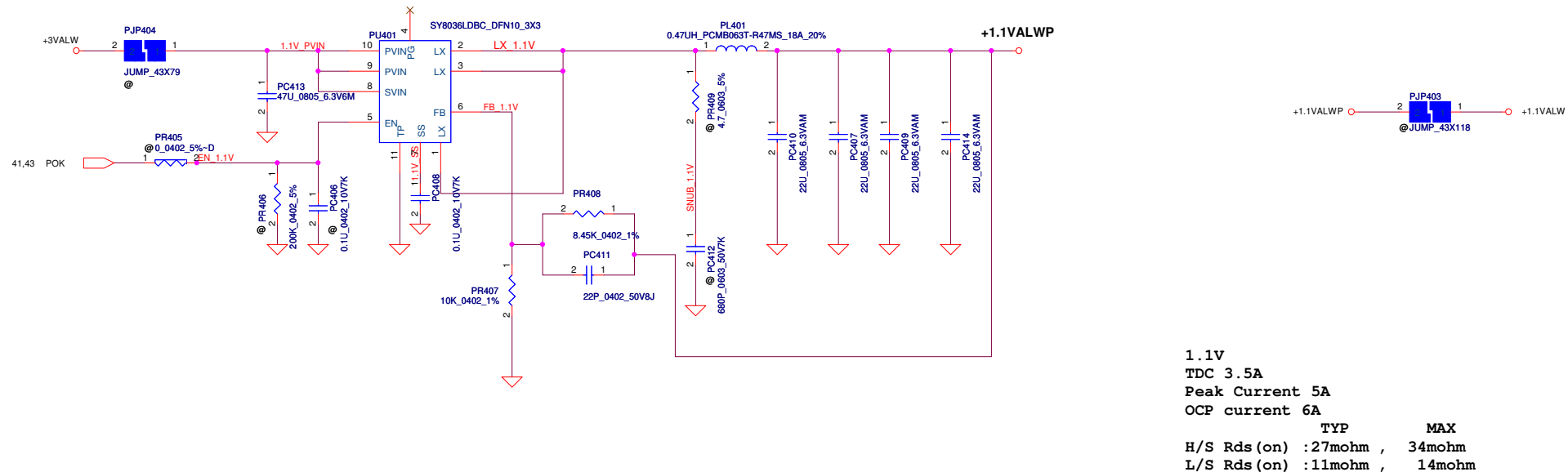
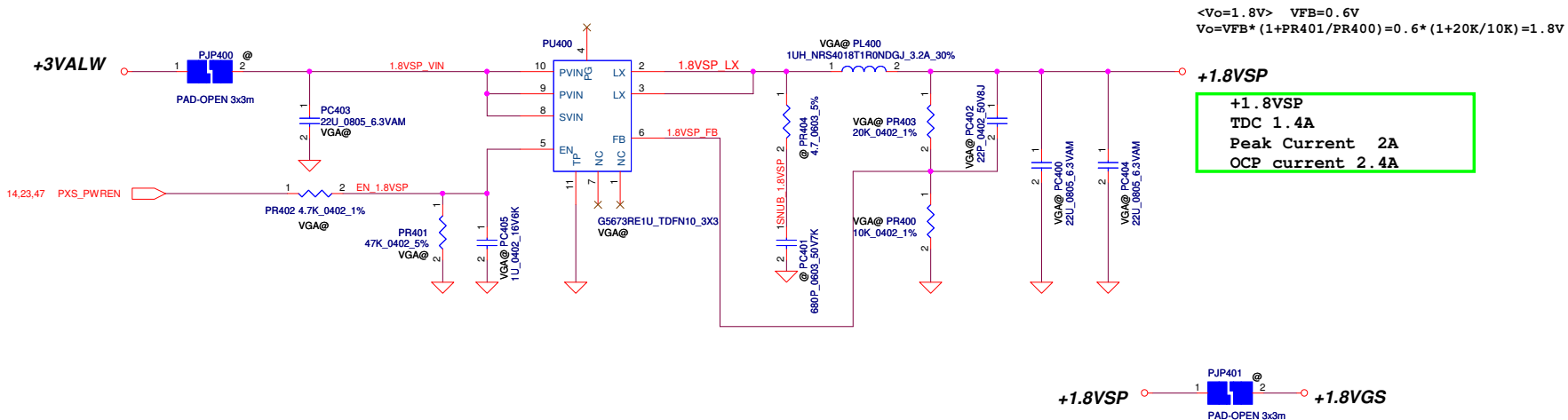
1.5VP
TDC 11A
Peak Current 16A
OCP current 19A

	TYP	MAX
H/S Rds(on)	: 23.2mohm	, 27.8mohm
L/S Rds(on)	: 7mohm	, 8.4mohm

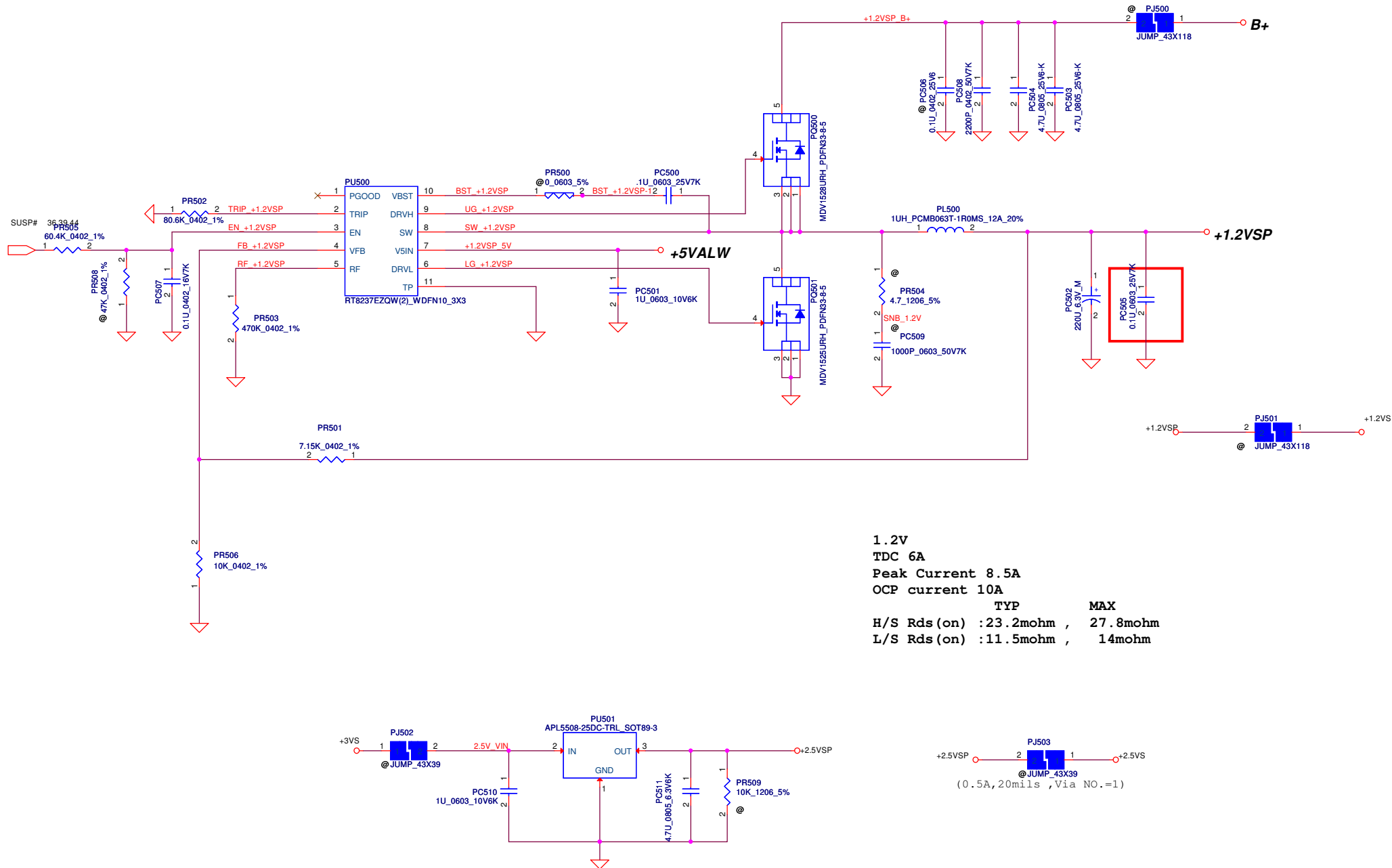
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

+1.5VGPU
TDC 5.6A
Peak Current 8A
OCP current 9.6A

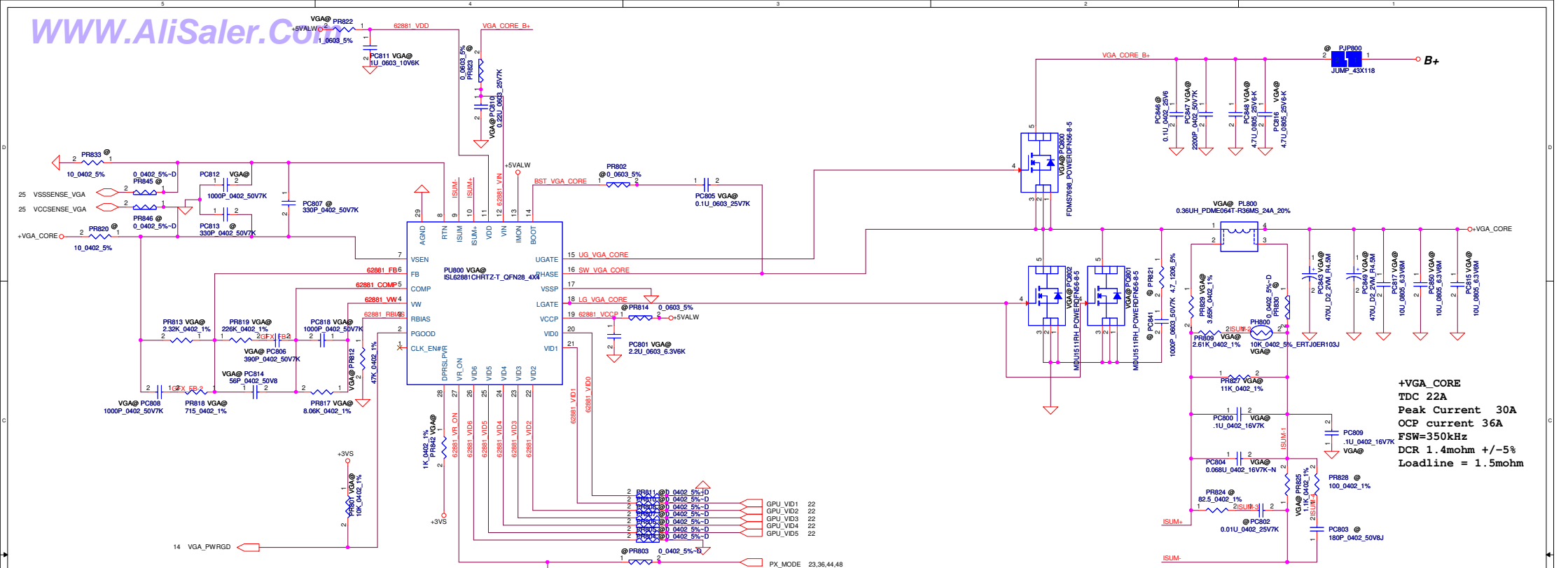
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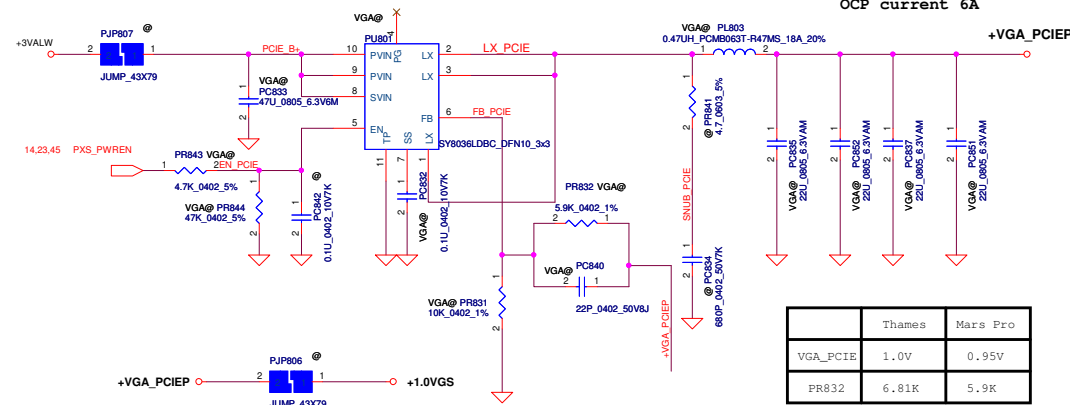
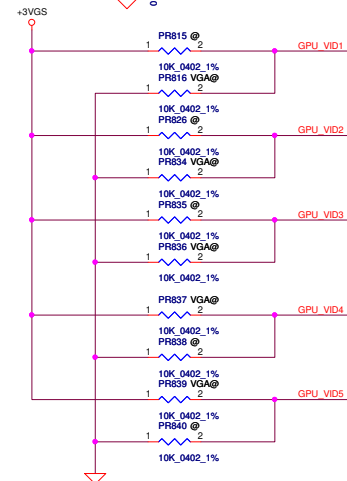


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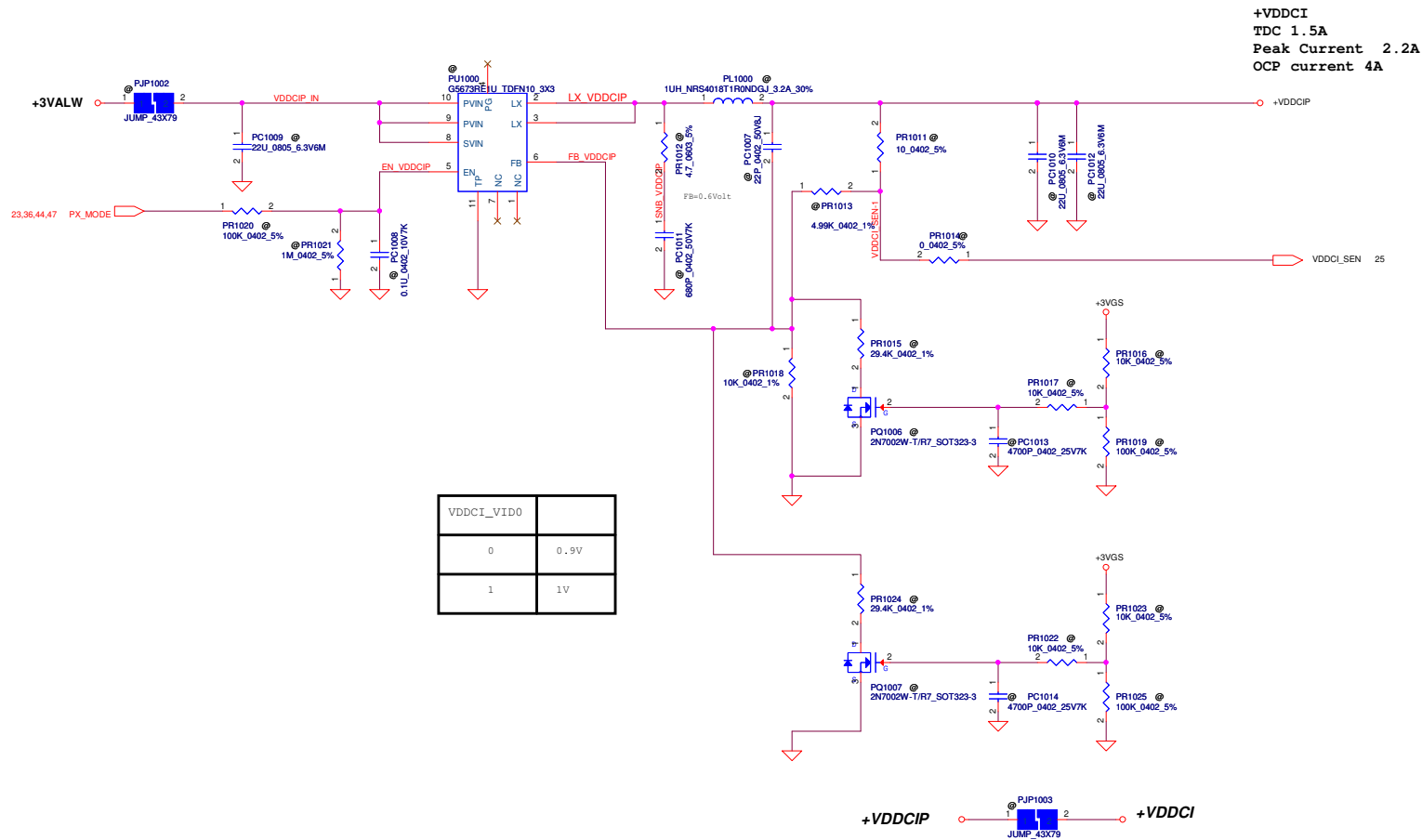


Mars Pro

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V



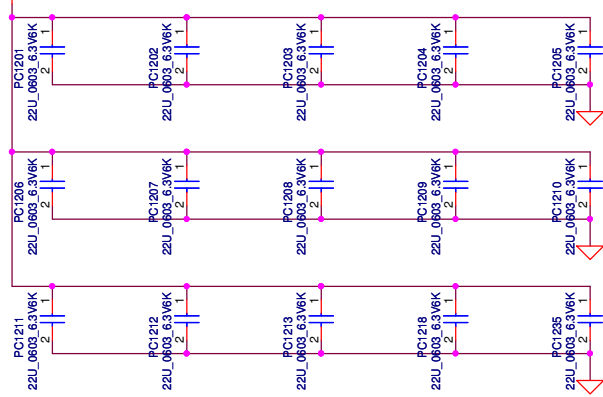
	Thames	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K



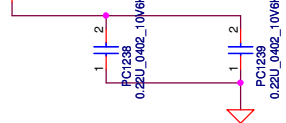


+APU_CORE

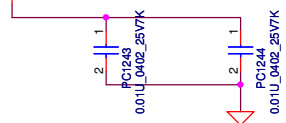
+APU_CORE



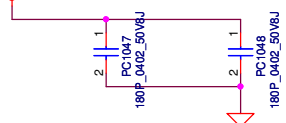
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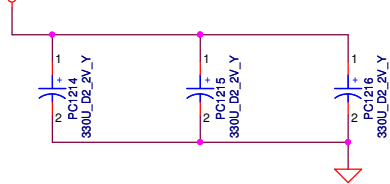
+APU_CORE



+APU_CORE

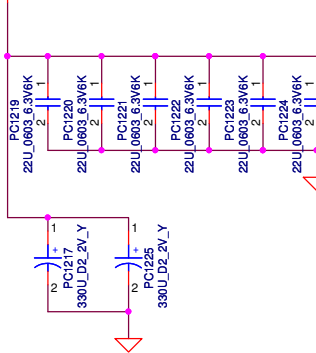


+APU_CORE



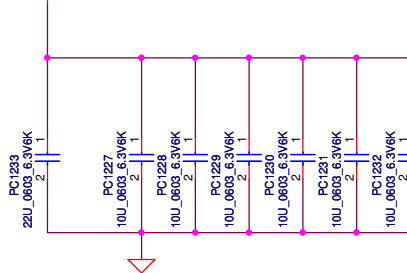
+APU_CORE_NB

+APU_CORE_NB



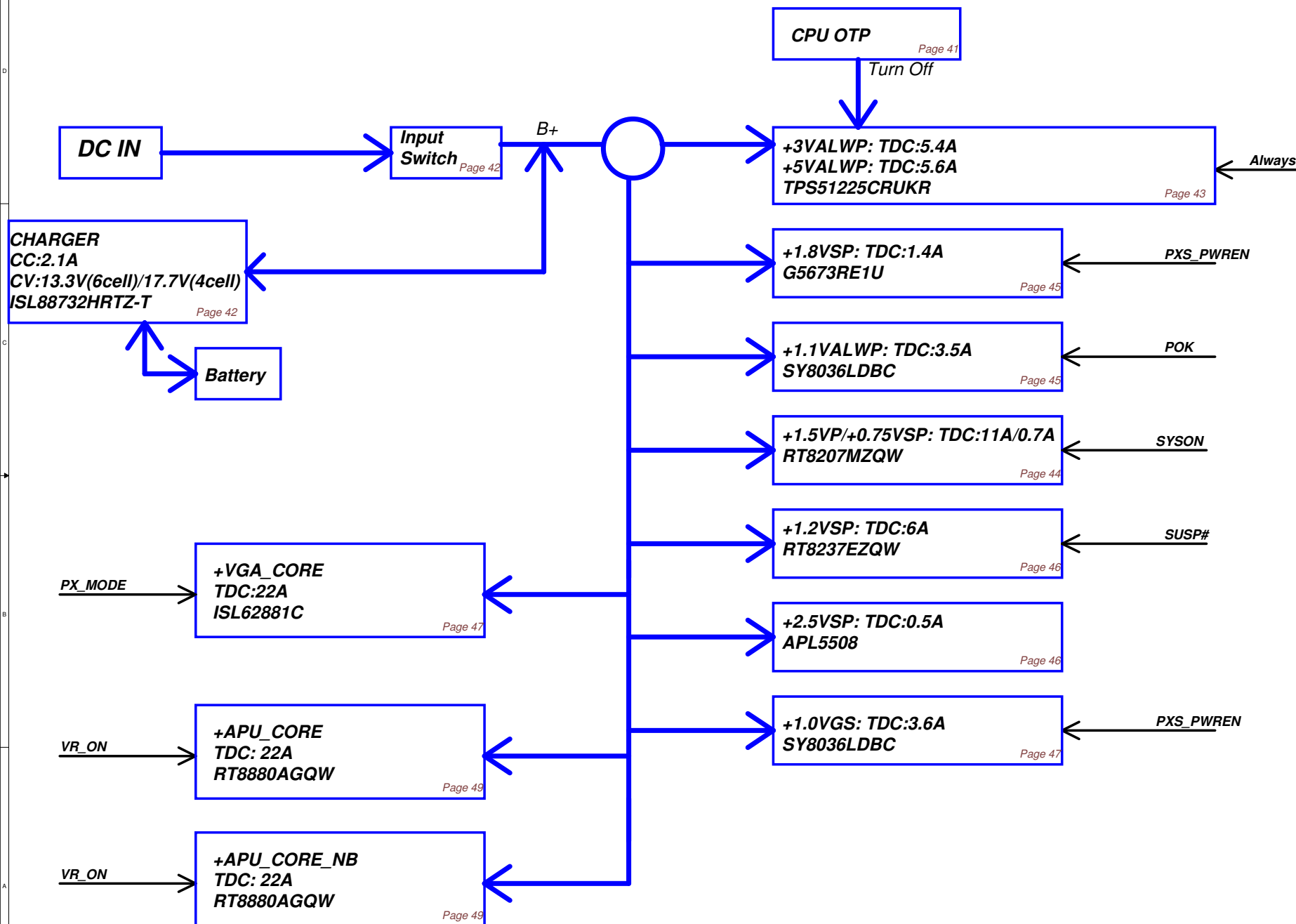
+1.2VS

+1.2VS



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Power block



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